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RECENT DEVELOPMENTS IN HVDC MODELING FOR THE RTDS SIMULATOR

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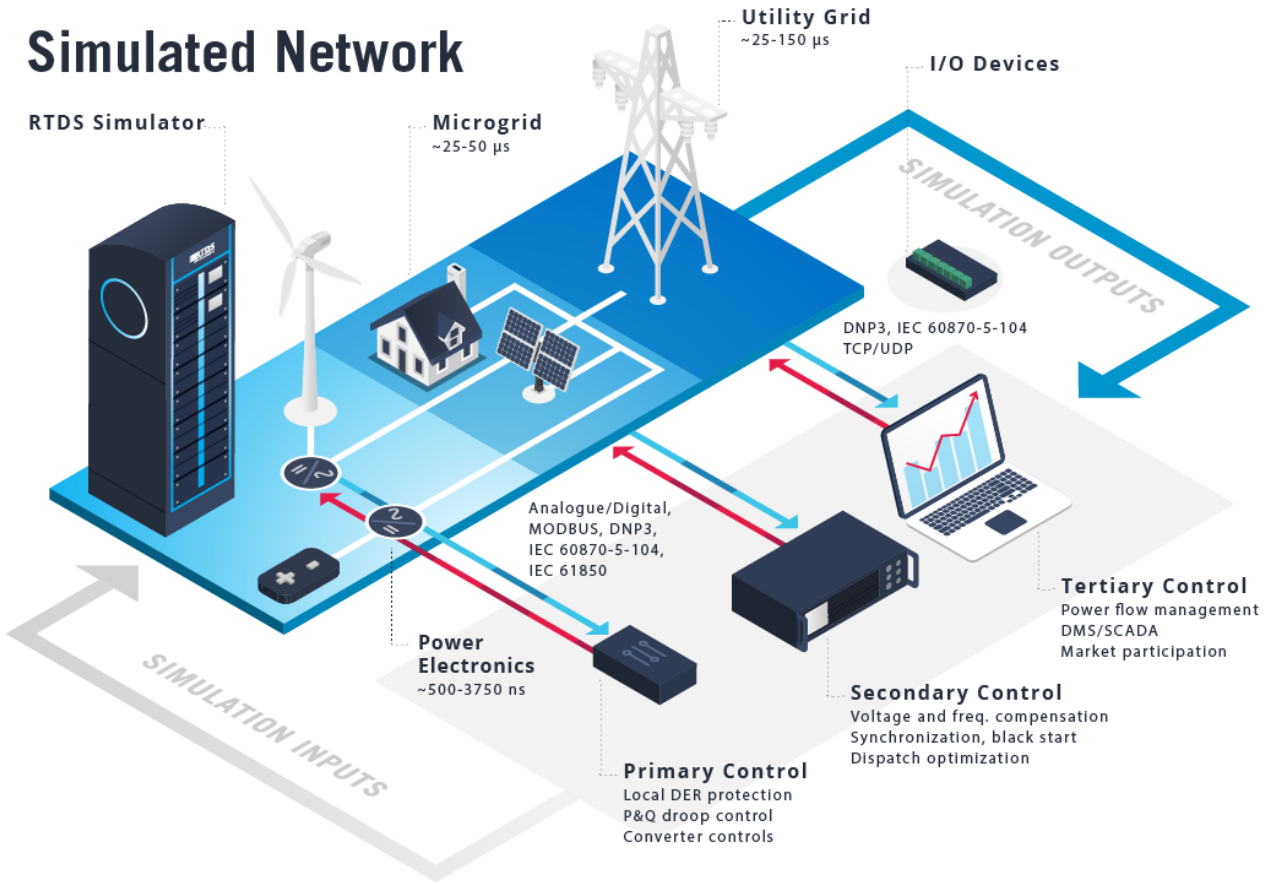
AGENDA

- New developments for renewables and energy storage
- Fully digital interconnection to P&C
- Vendor black box models
- Question and Answer Session
- Demo

RENEWABLES and ENERGY STORAGE

- Wind
- Solar
- Battery Energy Storage (BESS)
- Fuel cell
- Pumped hydro
- Flywheel



UNIVERSAL CONVERTER MODEL (UCM)

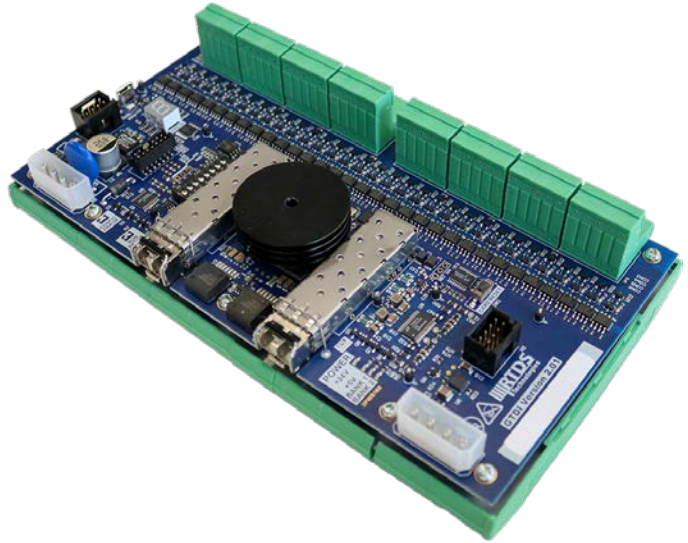
Renewables and energy storage are connected to the grid via converters

- **Investment made to develop more precise, versatile and robust model**
- **Multiple topologies supported**
  - 2-level, NPC (ANPC), T-type, boost and buck, flying capacitor, DAB topologies
- **Multiple input modes**
  - Modulation Waveform (essentially an average model)
  - Full Firing Pulse (reads firing pulse once per simulation timestep)
  - ***Improved Firing (with Mean Value High Precision)***
    - Captures firing pulses within a timestep at high resolution to calculate how much of the timestep the switch should be “on” (producing an effective duty cycle)
    - Multiple turn-on/turn-off transitions per timestep are allowed
    - 10 ns firing resolution
- **Available in Mainstep and Substep**
  - Mainstep allows 10 kHz PWM with 40 µs timestep
  - Substep allows 150 kHz PWM

UNIVERSAL CONVERTER MODEL (UCM)

Renewables and energy storage are connected to the grid via converters

- Other average model implementations decoupled on the DC bus – can cause instability
- UCM has no decoupling on the DC and does not use interface lines to connect to the network solution (i.e. the converter is embedded)
- Improved performance with a reduced computational burden
- External firing pulse control testing using GTDI v2 with 10 ns resolution



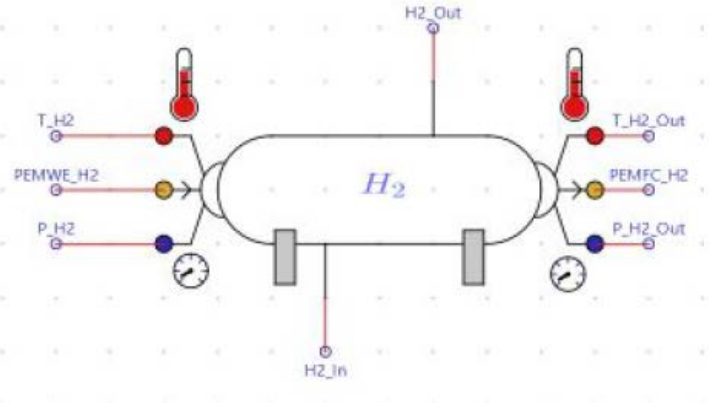
UNIVERSAL CONVERTER MODEL (UCM)

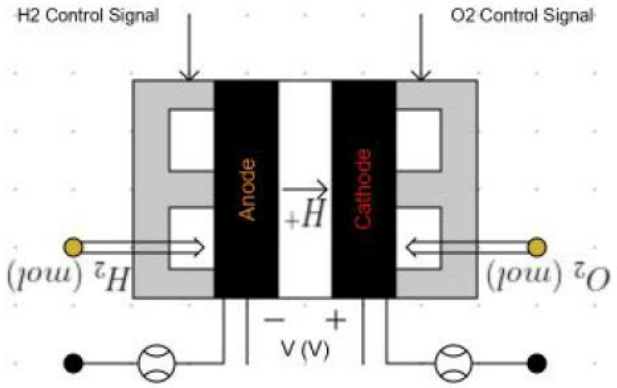
Benefits

- Use of resistive switching allows losses to be defined by the user
- Proper transitioning from blocked to deblocked states – UCM incorporates proprietary predictive switching technique from Substep models
- Improved Firing represents the characteristic harmonics very well and introduces minimal non-characteristic harmonics
- Good results even with a 30-50 us timestep – no need to maintain very small timesteps like other simulators which use decoupled models – fit many detailed converter models on a significantly reduced quantity of hardware

MULTI-ENERGY SIMULATION: HYDROGEN

- New electrolyser model created
- Hydrogen storage component to incorporate effect of inlet fluid temp and pressure
- Updated fuel cell component





FULLY DIGITAL CONNECTION TO P&C

- RTDS Technologies is working with HVDC and FACTS vendors to support fully digital interconnection of P&C to the RTDS Simulator

- Allow project testing to start earlier and reduce footprint and cost of replica simulators

- Protocols available or underdevelopment
  - Aurora
  - IEC 61850 GOOSE and MMS
  - IEC 61850 Sampled Values (including 96, 200 and 250 kHz)
  - DNP3 and IEC 60870-5-104
  - Modbus
  - EtherCAT (under development)

SUPPORT FOR VENDOR BLACK BOX MODELS

- Vendors need a mechanism to securely share proprietary models with 3rd parties
- Support for original code base is optimal
- Real time operation requires code to be compiled for the target platform
- DLLs created for offline simulation (e.g. PSCAD) cannot be used for real time
- RTDS Technologies has developed two solutions to support real time black box models

INTERVAL ZERO SOLUTION

Required by manufacturers to protect their IP

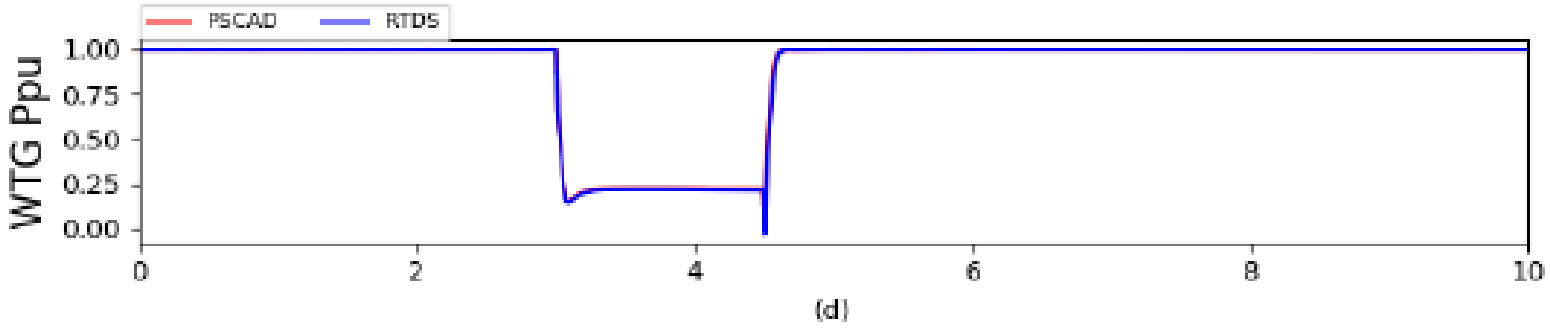
- **DLLs require MS Windows**
  - o Use Windows co-processing platform
- **Standard Windows OS suffers from substantial jitter**
  - o Not practical for hard real time simulation
- **Interval Zero offers a RTOS to work alongside Windows**
  - o Limitation is the code needs to be compiled using Interval Zero software or Statically Linked Libraries are required
- **Direct Ethernet link using NovaCor UDP port**
  - o Optimized communication techniques utilized

Direct UDP link

IntervalZero

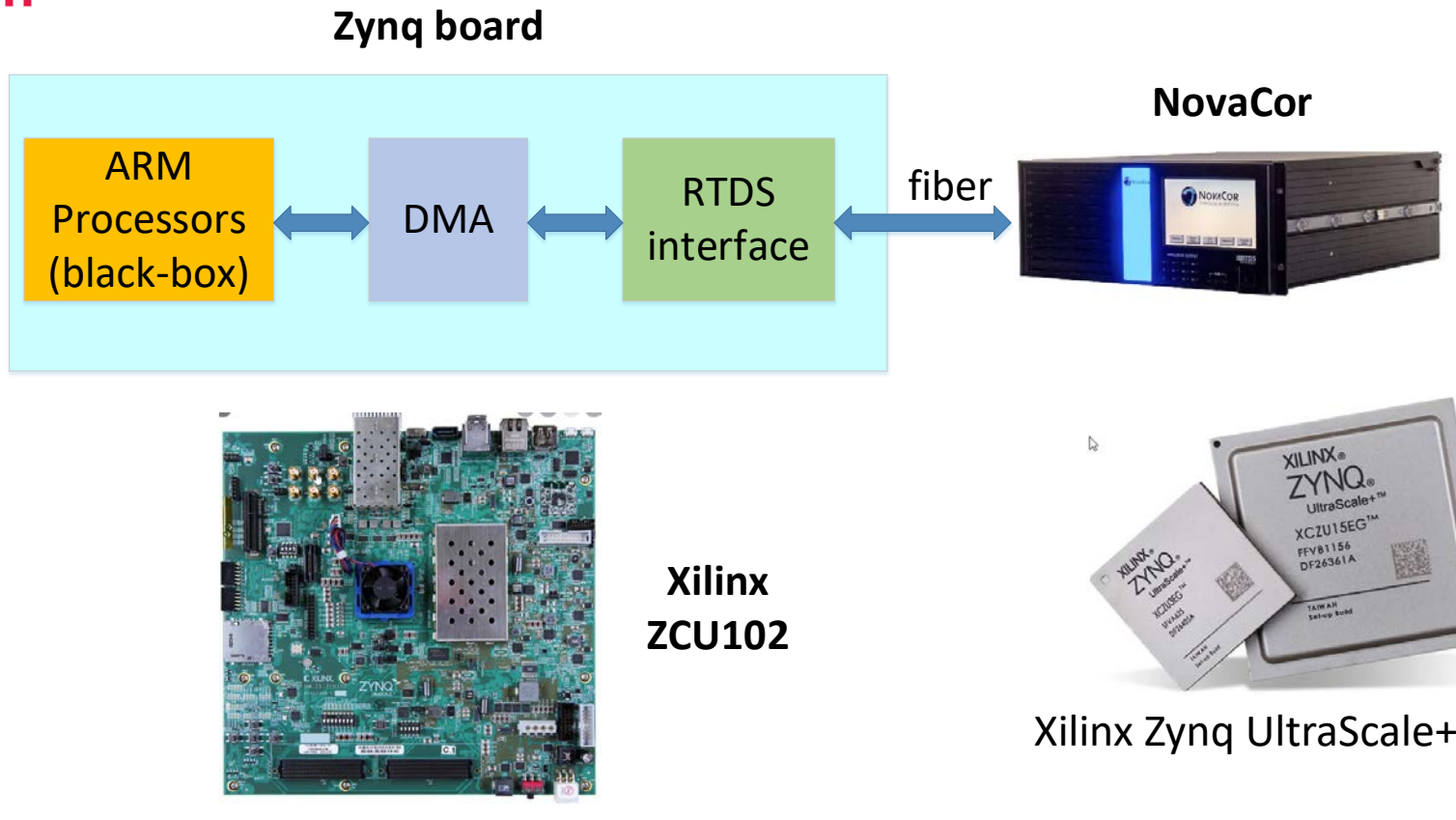
INTERVAL ZERO SOLUTION

- Integrated Vestas control DLL into RSCAD – proof of concept for any manufacturer's black box control DLLs
- Implemented 1 PPC and 4 wind turbine controllers communicating with the RTDS Simulator
- Excellent comparison to PSCAD
- User Spotlight Series recording available with presentation from Vestas



ZYNQ – ARM CORE SOLUTION

Second solution



Xilinx ZCU102

Xilinx Zynq UltraScale+ MPSoC

Note: Xilinx ZCU102 for experiment
Custom board coming soon

ZYNQ – ARM CORE SOLUTION

? **Linux OS on Zynq board running Dynamic library (.so)**

The problem is the undeterministic execution time spike ~ 200 us, hard to eliminate without specialized real-time Linux OS support.

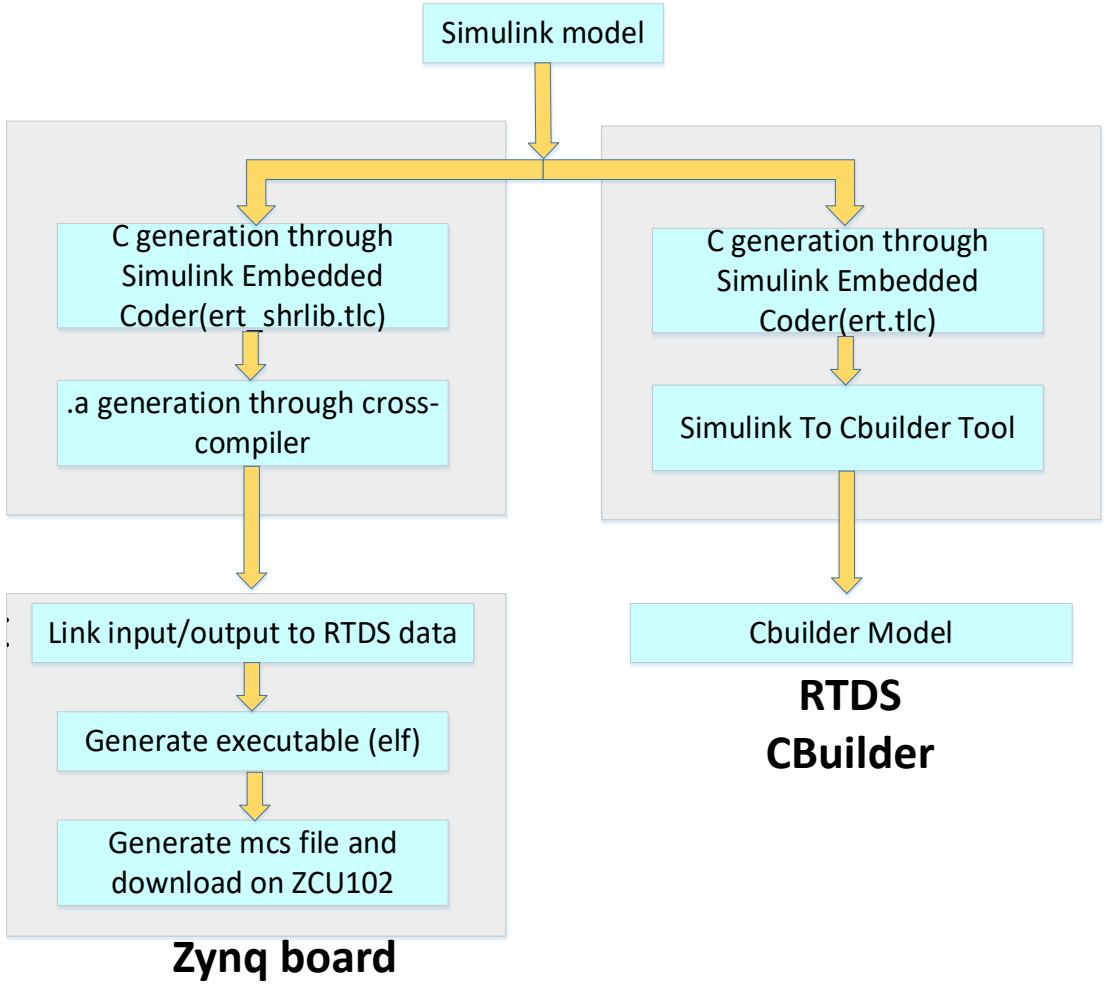
✓ **Bare metal on Zynq board running Static library (.a)**

Bare metal guarantees deterministic timing: <1us jitter.

ZYNQ – ARM CORE SOLUTION

Procedure using Simulink

- A batch file is provided to compile the C code generated from Simulink. This batch file can automatically generates the required .a and .so files.



ZYNQ – ARM CORE SOLUTION

Procedure directly from C code or C++ using GNU cross-compiler

- Two batch files are provided for generating .a and .so files
  - One for general C
  - One for general C++

```
Microsoft Windows [Version 10.0.16299.2166]
(c) 2017 Microsoft Corporation. All rights reserved.

D:\ZCU102\mycontroller>compile_C.bat mycontroller
VERSION: 1.0    |       2021-10-01      |       COPYRIGHT (c) RTDS TECHNOLOGIES INC. 2021

BUILDING FILES: "*.c"
BUILDING TARGETS: "*.o"
INVOKING: ARM V8 GCC BARE-METAL (.a) COMPILER

COMPILING D:\ZCU102\mycontroller\test.c

ARM V8 GCC BARE-METAL (.a) COMPILER SUCCESSFUL

BUILDING FILES: "*.o"
BUILDING TARGET: "libmycontroller.a"
INVOKING: ARM V8 BARE-METAL (.a) ARCHIVER

ARM V8 BARE-METAL (.a) ARCHIVER SUCCESSFUL

DELETED "D:\ZCU102\mycontroller\test.o"

BUILDING COMPLETE, FILE: "libmycontroller.a"

BUILDING FILES: "*.c"
BUILDING TARGETS: "*.o"
INVOKING: ARM V8 GCC LINUX (.so) COMPILER

COMPILING D:\ZCU102\mycontroller\test.c

ARM V8 GCC LINUX (.so) COMPILER SUCCESSFUL

BUILDING FILES: "*.o"
BUILDING TARGET: "libmycontroller.so"
INVOKING: ARM V8 GCC LINUX (.so) LINKER

ARM V8 GCC LINUX (.so) LINKER SUCCESSFUL

DELETED "D:\ZCU102\mycontroller\test.o"

BUILDING COMPLETE, FILE: "libmycontroller.so"

PREPARING OUTPUT FOLDER
COPYING FILES

D:\ZCU102\mycontroller\rtds.h -> D:\ZCU102\mycontroller\TO_RTDS\rtds.h
1 File(s) copied
D:\ZCU102\mycontroller\libmycontroller.a -> D:\ZCU102\mycontroller\TO_RTDS\libmycontroller.a
1 File(s) copied
D:\ZCU102\mycontroller\libmycontroller.so -> D:\ZCU102\mycontroller\TO_RTDS\libmycontroller.so
1 File(s) copied

FILES COPIED TO "D:\ZCU102\mycontroller\TO_RTDS", please zip all files and send to RTDS Technologies Inc. Thank you.
```

ZYNQ – ARM CORE SOLUTION

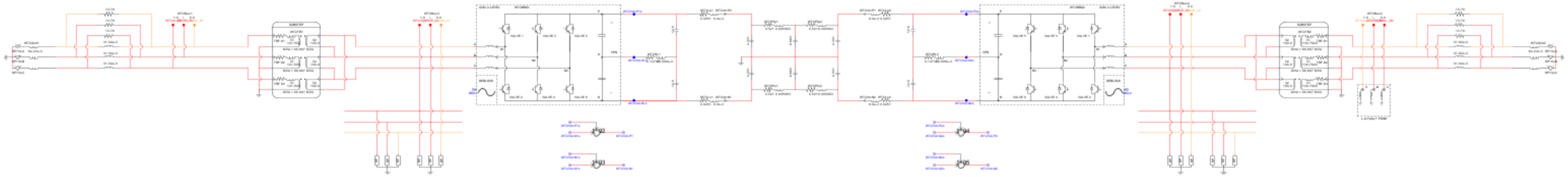
Testing

- Test Scenarios
  - Single static library on Zynq
    - ✓ STATCOM
    - ✓ VSC-HVDC
  - Multiple static library on Zynq
    - ✓ STATCOM+VSC-HVDC
  - Single static library with multiple instances on Zynq
    - ✓ Two STATCOM Instances
  - Synchronous mode: Static Library simulation step size is set by users. RTDS simulation timestep must be the same as used to create the static library.
  - Asynchronous mode: Static Library simulation step size is set by users. RTDS simulation timestep could be set independently.

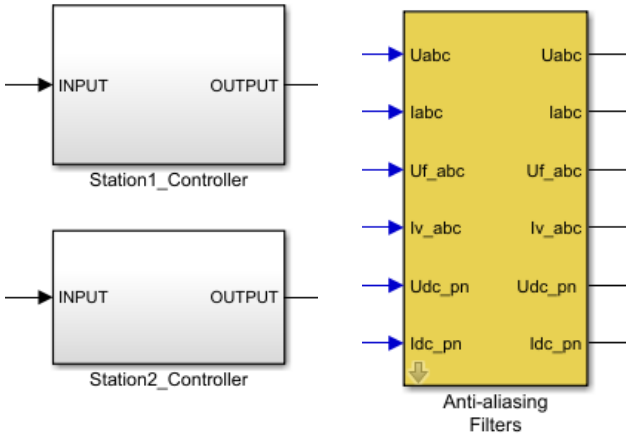
ZYNQ – ARM CORE SOLUTION

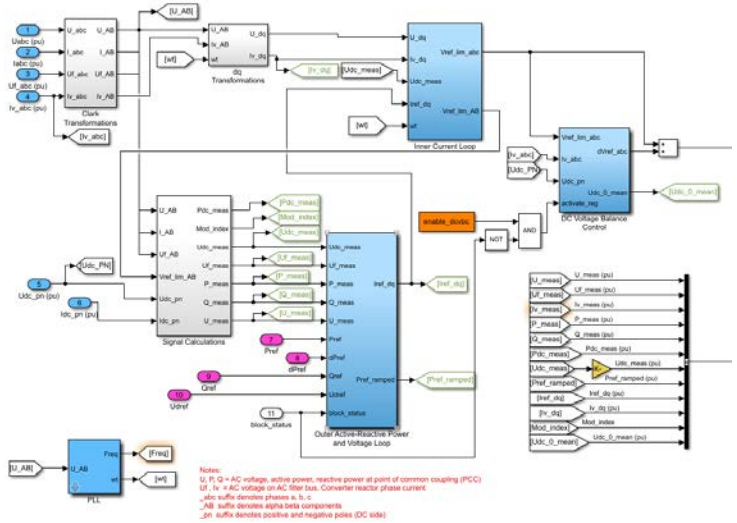
Testing – VSC Based HVDC Case

- Power System Circuit:



- Control Systems:
  - Two Station Controllers
  - Each Station includes:
    - Anti-aliasing Filters
    - Outer-loop controller
    - Inner-loop controller
    - DC Voltage Balance
    - Others

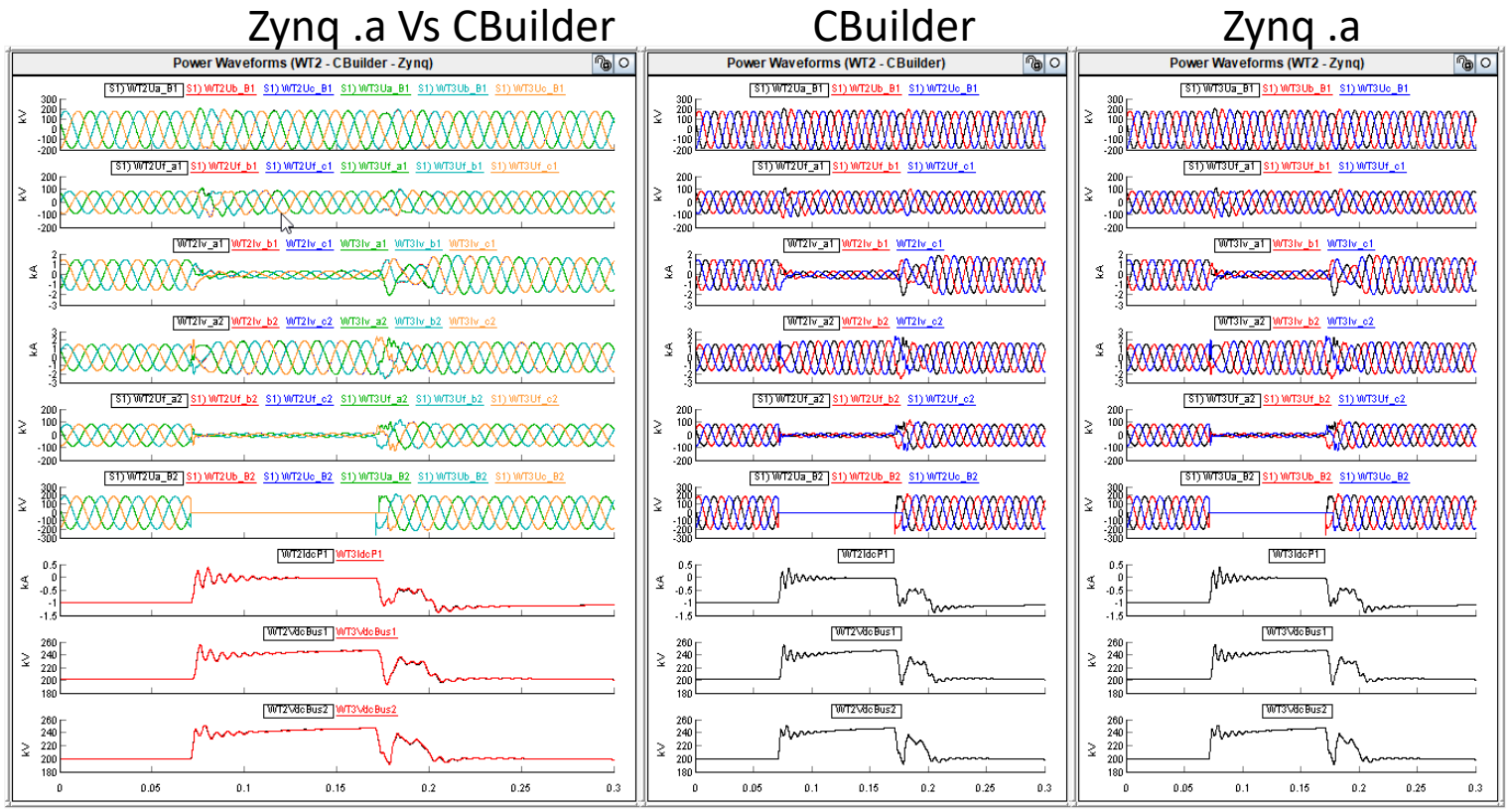




- Reference Simulink case: power_hvdc_vsc.slx

4 Testing

4.4 Test Results: VSC-HVDC



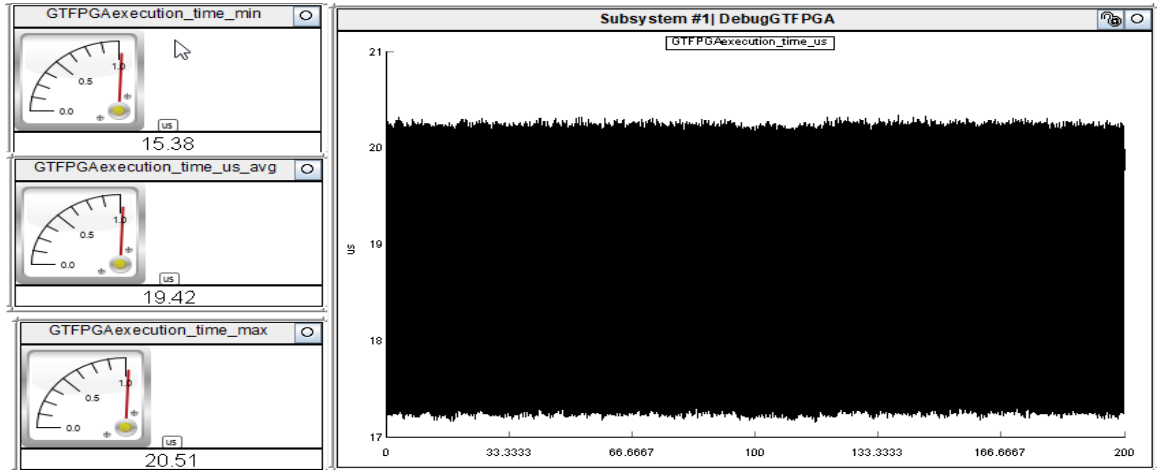
3-phase ac grounding fault in Station 2

ZYNQ – ARM CORE SOLUTION

Testing – Timing

Test Case	Timing (Average, us)
STATCOM + Interface	13.55
(VSC-HVDC) + Interface	11.48
STATCOM + (VSC-HVDC) +Interface	19.42

Test Case	Timing (Average, us)
STATCOM*N	7.94*N
VSC-HVDC	5.74
Interface	5.87



Timing Measurement for Multiple Static Library (STATCOM + VSC-HVDC)

THANK YOU!
QUESTIONS?

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