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Optimal control setting and PLL types with improved technical specifications considering grid strength for the stable operation of HVDC's in the GB system.	Issue: Date

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Executive Summary

The report is made in response to the agreement between National HVDC Centre and Cardiff University on the Grid Code Compliance project. This report evaluates the sensitivities of system parameters, particularly the varying grid strength, impact of PLL design, reactive current limit and recovery rates after fault for HVDC-connected to strong and weak networks. Specific focus has been made on the existing codes in relation to these system parameters from the GB Grid Code requirements.

PSCAD/EMTDC transient analysis tool is used to model relevant test system components and HVDC systems to extend the sensitivity assessment on a simulation environment. With the input of the National HVDC Centre, systematic test method for mitigation of unstable conditions at low system strength conditions are developed in PSCAD and aggregated to test different grid strength and future energy scenarios. HVDC schemes involving different convertor control configurations, PLL topologies and fault ride through (FRT) schemes are also developed for testing. The models developed in this task will be utilised in Task 2 to perform grid code compliance tests and developing fast fault current injection methods. These optimal settings for low SCR can then be tested again in EMT to check they are robust at max SCR conditions.

Identification of a systematic test method for mitigation of unstable conditions at low system strength conditions in EMT platform is provided with relevance to existing GB Grid Code. Summary of sensitivity studies with respect to reduced system strength and operation of HVDC with different PLL types are included and connected to the existing Grid Code requirements. The requirements of specifications for stable HVDC connection to weak grids are tested for the most onerous case, the fault ride through case with respect to the HVDC convertor capability.

For validation purpose the analysis performed in EMT platform is implemented as a real-time hardware-in-the-loop configuration. The AC grid is modelled in RSCAD/RTDS to represents different grid strength by varying the impedance. An HVDC test rig with DC link in physical platform is used to close the loop and perform the FRT test. Results agrees well with the simulation validating instability and inability of voltage to recover when connected to a weak grid operation after a severe fault. Based on these analysis best practice recommendations for HVDC operation connected to weak grid is provided.

Nomenclature

AC	Alternating Current
APF	All Pass Filter
CM	Caithness-Moray
DC	Direct Current
DSOGI	Dual Second Order Generalized Integrator
ENTSO-E	European Network of Transmission System Operators for Electricity
FRT	Fault Ride-Through
GB	Great Britain
HVDC	High Voltage Direct Current
MMC	Modular Multi-level Convertors
MW	Mega Watts
MVA	Mega Watt Ampere
NF	Notch Filter
NC	Network Code
PLL	Phase Locked Loop
PI	Proportional Integral
PCC	Point of Common Coupling
SS	State Space Optimised
SCR	short-circuit ratio
SCL	Short Circuit Level
SRF	Synchronous Reference Frame
VSC	Voltage Source Convertor
VCC	Vector Current Control

1. Introduction

As the dynamics of the power electronics equipment's used in HVDC connections are mainly dictated by the assigned controllers, all the parts of a typical control strategy of the VSC needs to be studies in detail for grid code compliance tests [1]. First and foremost, the phase-locked loop (PLL), a popular grid voltage synchronization technique, is investigated and tested for weak gird scenario in an embedded link. However, a VSC-HVDC connected to a weak ac system is still facing the problem of PLL synchronisation. A weak ac system has two major characteristics, i.e. high impedance of ac system and low mechanical inertia relative to dc power infeed that is shown as smaller short-circuit capacity (SCR) and lower inertia constants [2]. These two characteristics are caused by the expansion of power grids and increased penetration of renewable energy generation, respectively. When a VSC-HVDC is connected to a weak ac system, the variation of power transmission is highly sensitive to the voltage magnitude and frequency at the point of common coupling (PCC). Several control methods have been introduced and proposed in the recent times for mitigating this impact. However, majority of VSC based connections still uses vector current control (VCC) strategy that uses an enhanced outer loop based on a decoupled and inner current controller to overcome the non-linearity of the active power and voltage interactions synchronised by PLL

In this regard, the different types of PLL and their usage in varied applications has been of importance. The synchronisation of power convertors to the connected grid largely depends on the robustness of these devices. To this end, the performance of different types of PLL's: the Synchronous Reference Frame (SRF)-PLL, the Notch filter (NF- PLL), the Dual Second Order Generalized Integrator (DSOGI)-PLL, State Space Optimised (SS-PL) and All Pass Filter (APF-PLL) are studied and critically compared when subjected to a severe grid fault [3-4]. It is shown that the DSOGI-PLL gives the best performance when compared to the SRF-PLL, the traditional one, as identified from the literature and has shown a strong potential to offer better performance under transient grid events [3]. This is of significant specification when considering Grid Code compliance especially during defining Fault Ride Through requirements. To this end during different contingencies, interactions with grid and HVDC circuit behaviour plays a critical role in stability and for devising grid codes, especially for weak grid. This is what is presented in this report.

1.1 Test System Configuration

The system under investigation is shown in Figure. 1. The system resembles that of an embedded HVDC link within a synchronised grid, built to enable around 1,200 MW of additional renewable capacity to connect to the electricity network. The link uses half-bridge modular multi-level convertors (MMC) HVDC technology to transmit power through a 113 km subsea cable between convertor stations representing 1 and 2. The grid 1 has relatively weak system characteristics, with a wide range of system strengths, with generation at the area dominated by onshore wind. To put in the context, it has been identified that the system strength at the point of common coupling (PCC) of the HVDC link embedded in the GB system can vary from 1 to 5 GVA over the lifetime of the project [8]. To further evaluate the test system, the details and operating modes are outlined in Table 1. A conservative yet reasonable assumption on the parametrisation is used for modelling the test system. This includes, selection of grid strength of Grid2, HVDC topology, tuning of the MMC controllers. Moreover, the HVDC link model has been widely used by industry under the assumption that it accurately represented the installed equipment in practice.

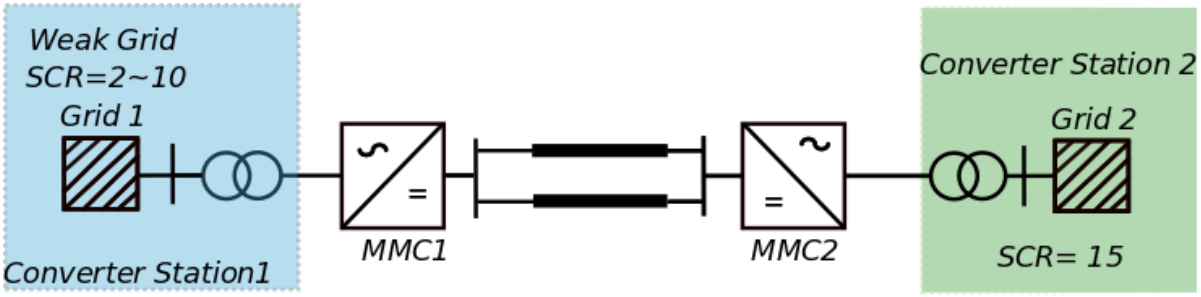


Fig. 1. Embedded HVDC link configuration

Table 1 Embedded HVDC link operating Modes

Item	MMC1	MMC2
Rated Apparent Power (S)	840 MVA	1265 MVA
Rated Active Power (P)	±800 MW	±1200 MW
Convertor DC Voltage	640 kV (±320 kV)	
AC Grid Voltage	275 kV	400 kV
SCR	2~10	15
Transformer Reactance	0.16 p.u.	0.16 p.u.
Control Mode	P and Q (CM1) P and Vac (CM2)	Vdc and Q

2. Grid Strength and HVDC connection requirements with Different PLL Design

The testing of HVDC operation and performance with varying grid strength corresponding to different PLL design is undertaken and reported in this section. These PLL designs were adapted from an NIA project-NGSO_0005-NIA [3]. Five differed PLL models were developed in PSCAD to facilitate convertor connection to system with varying strength.

2.1 The different PLL models

A summary of different PLL designs reported in the NIA study is provided below and is included in Table 2. For more information the readers are referred to [3]

1) Synchronous Reference Frame (SRF-PLL)

- classical/ standard approach
- minimises balanced phase error

2) Notch filter (NF- PLL)

- overcomes negative phase sequence limitations;
- filter centred on 100Hz

3) All Pass Filter(APF-PLL)

- alternate approach
- tuned in alpha-beta frame.

4) Double Second Order Generalised Integrator (DSOGIPLL)

- doubly filtered; more complex,
- inherently slowed and smoothed response

5) State Space Optimised (SS-PL)

- require complex definition of network
- dynamic state space, normally not available

Table 2 summaries the PLL models implementation in different applications with respect to performance and design complexity. We used this summary and implemented all the PLL's for HVDC convertors operating in different grid strength to find the optimal setting when connected to system with varying grid strength and subjected to severe ac fault.

Table 2 PLL Types with application [3]

Description	Design	Expected Performance	Application
SRF-PLL	Simple	Poor	Small generators
NF-PLL	Average	Average	HVDC, Large Generators
APF-PLL	Average	Average	HVDC, Large Generators
DSOGI-PLL	Average	Good	Large Generators

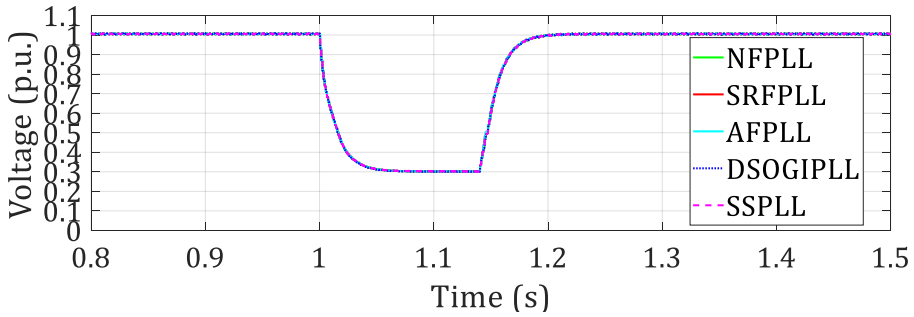
3. Grid Code connection testing with different PLL subjected to severe fault and varying Grid Strength

The testing of HVDC operation and performance with varying grid strength under the most onerous stability test, the FRT corresponding to different PLL design is undertaken and reported in this section. These aligns with the FRT compliance against requirements ECC.6.3.15 detailed in ECP.A.3.5 and ECP.A.6.7 of the GB Grid Code [8]. PSCAD/EMTDC transient analysis tool is used to model relevant test system components and HVDC systems to extend the sensitivity assessment on a simulation environment. The design of PLL and its impact, especially on the normal, fault and post fault operation of the HVDC link connected to AC grid is a critical requirement in all the Grid Codes and is therefore evaluated in detail in the following sections.

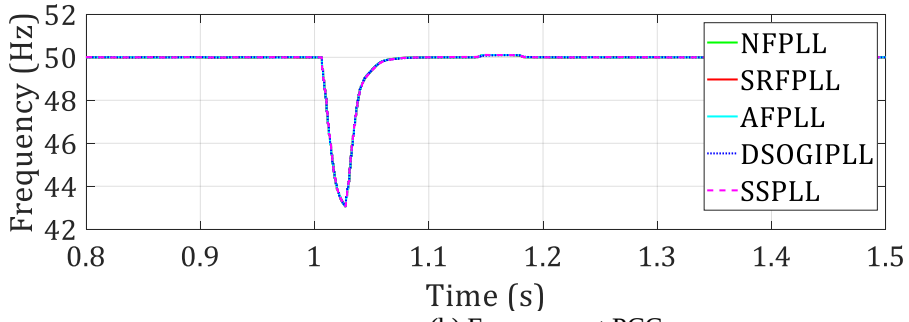
3.1 Case Study 1: FRT Performance of HVDC connection to Strong Grid with different PLL

A case was performed for SCR=40 with five PLL types and fault to understand how HVDC performance change under fault for a strong grid with different PLL types. As shown in Figure 2, at *t=1* s a three-phase symmetrical fault is applied at grid 1 for 140ms. Fault impedance is selected to retain 30% voltage at PCC during fault. DSOGI and SS based PLL tracks the frequency during fault while others hit the limits. SS PLL takes long time to settle after the fault recovery.

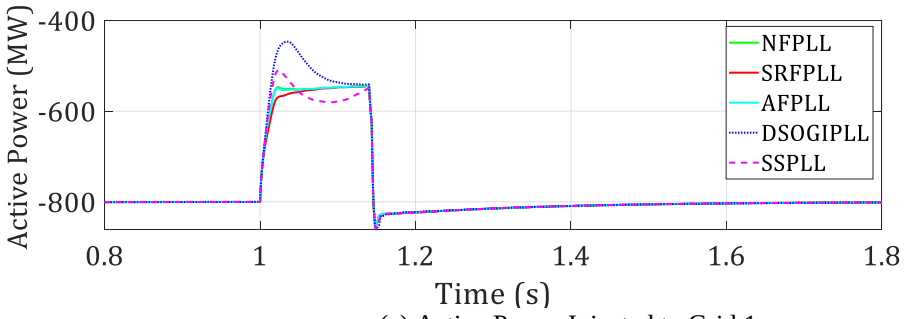
Active power during the fault reduces and the minimum value varies for different PLL types, as depicted in Figure 2(c). No P/Q priority or fast fault current injection is considered for this case. From the results it can be concluded that voltage support through reactive power can be provided with all PLL types when the HVDC is connected to s very strong grid without any control setting update irrespective of PLL types. However, the reactive power recovery after fault takes more time when different synchronisation methods are applied.



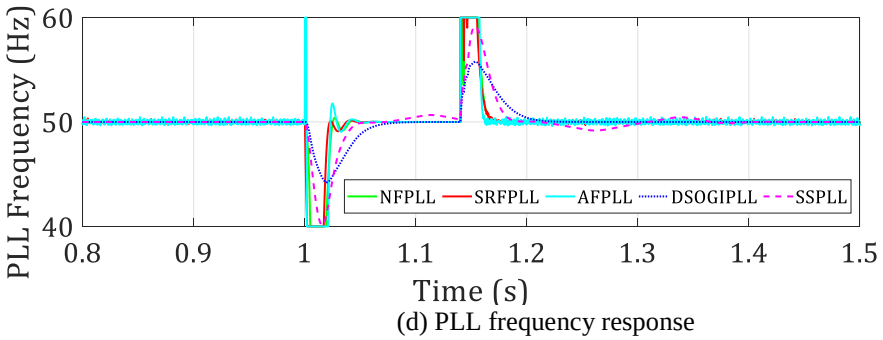
(a) Voltage at PCC



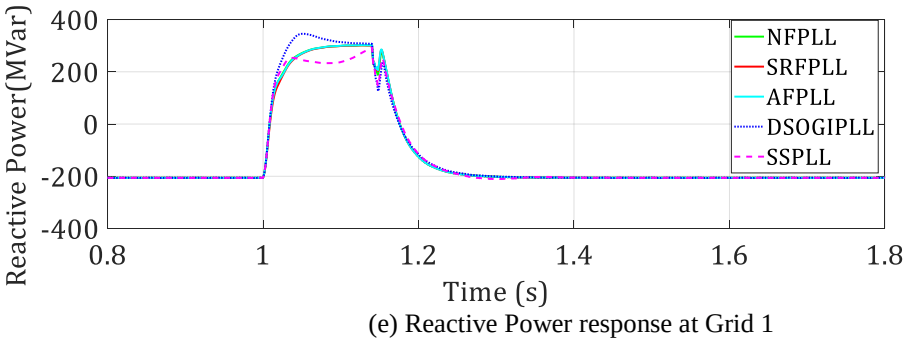
(b) Frequency at PCC



(c) Active Power Injected to Grid 1



(d) PLL frequency response



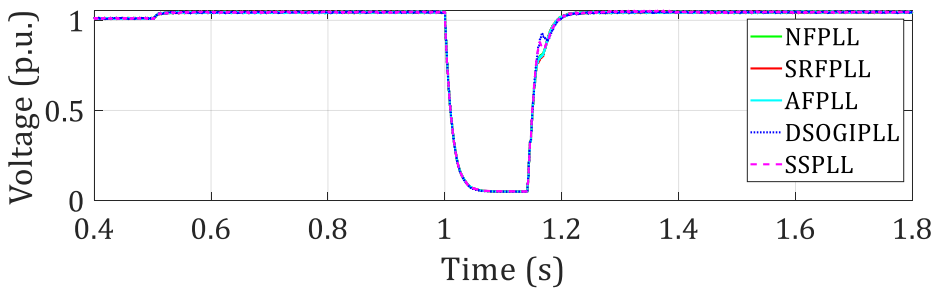
(e) Reactive Power response at Grid 1

Figure 2 FRT Response for Strong Grid (SCR=40)

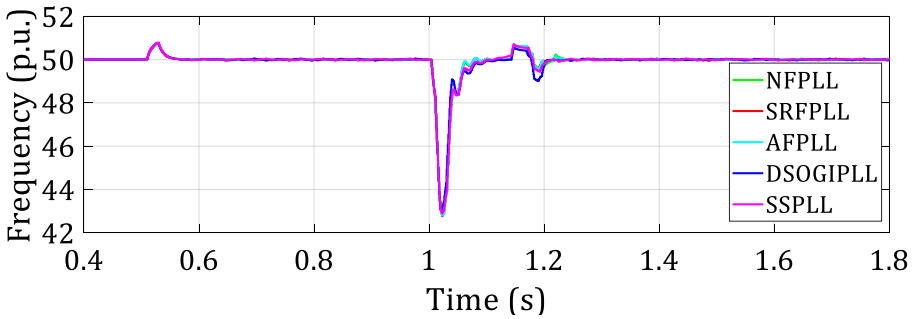
3.2 Case Study 2: FRT Performance of HVDC connection to Marginally Weak Grid with different PLL

This case analyses the HVDC performance change under fault for a relatively strong grid with different PLL types. As shown in Figure 3, at *t= 0.5 s* the grid impedance is changed to emulate SCR=5 operation and at *t=1s* a three-phase symmetrical fault is applied at AC grid 1 for 140ms. Fault impedance is selected to retain 30% voltage at PCC during fault as previous case, however, can't retain the PCC voltage but recovers after fault. DSOGI and SS based PLL tracks the frequency during fault while others hit the limits and oscillates from the steady state value as seen from Figure 3(d).

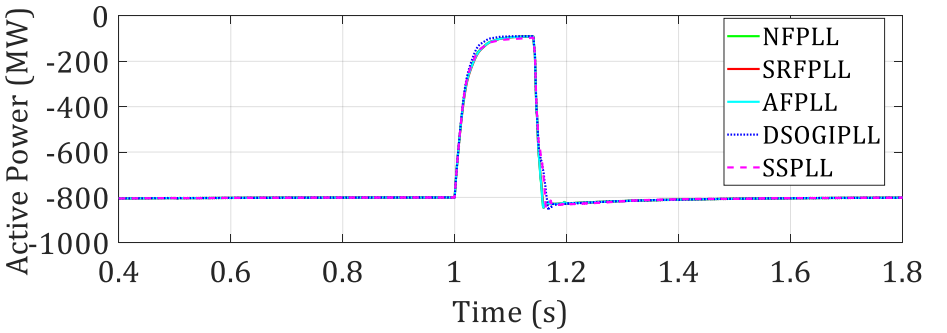
Active power during the fault reduces corresponding to the PCC voltage dip, as depicted in Figure 3(c). For the case studied here no P/Q priority or fast fault current injection is considered. Voltage support through reactive power can be provided with all PLL types for the marginally strong grid under severe fault case. Phase angle jump during the impedance change and fault can be observed but return to the pre-disturbance value as shown in Figure 3(f).



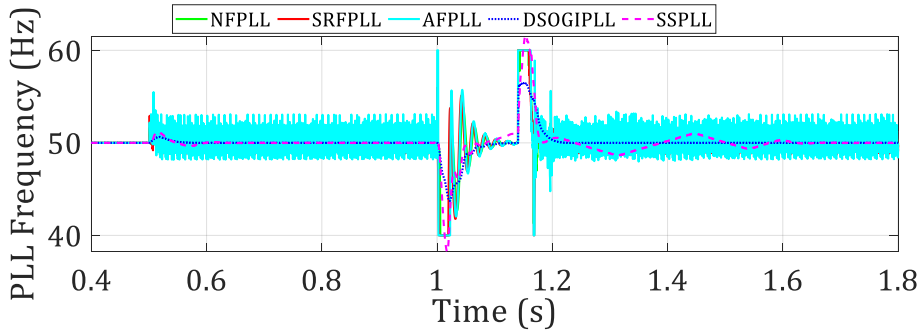
(a) Voltage at PCC



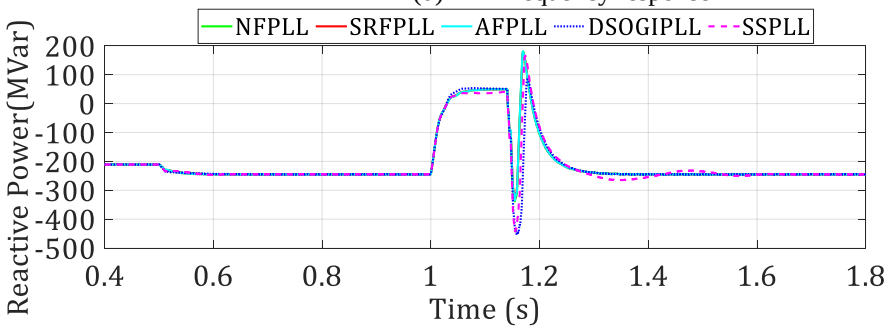
(b) Frequency at PCC



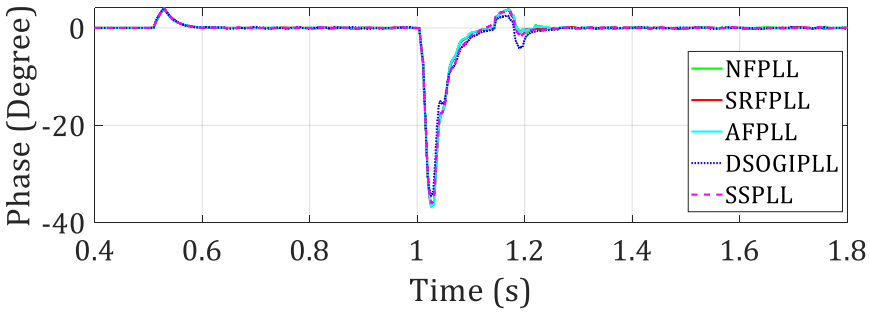
(c) Active Power Injected to Grid 1



(d) PLL frequency response



(e) Reactive Power response at Grid 1



(f) Phase response at PCC

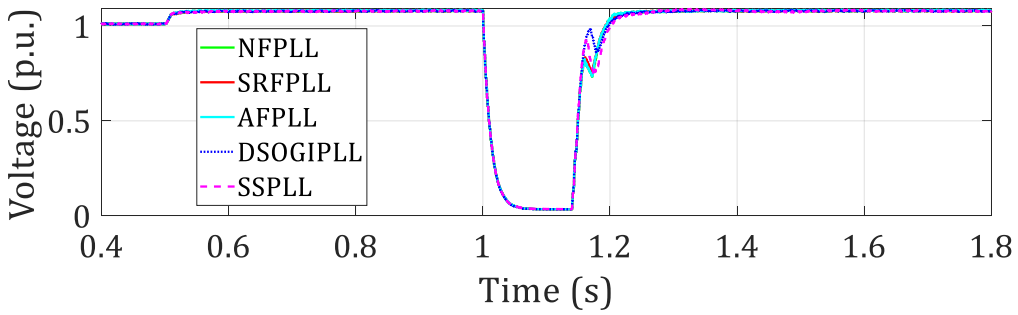
Figure 3 FRT Resposne for Marginally Weak Grid (SCR=5)

3.3 Case Study 3: FRT Performance of HVDC connection to Weak Grid with different PLL

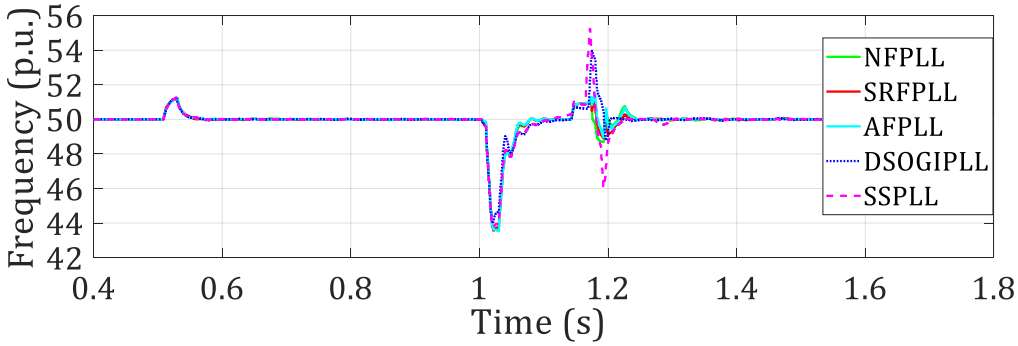
With reduced system strength how does the HVDC performance behaves under fault with different PLL types is studies through this case. As depicted in Figure 4 at *t= 0.5 s* the grid impedance is changed to emulate SCR=3 operation and at *t=1s* a three-phase symmetrical fault is applied at AC grid 1 for 140ms. Fault impedance is selected to retain 30% voltage at PCC

during fault as previous case, however, can't retain the PCC voltage but managed to recover after fault as shown in Figure 4(a). However a second dip occurs during the recovery period. Only DSOGI PLL tracks the frequency during fault while others hit the limits and oscillates from the steady state value with increasing magnitude as seen from Figure 4(d).

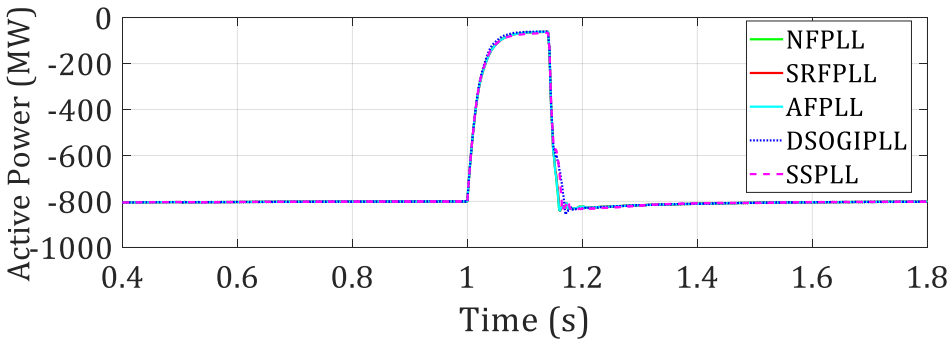
Figure 4(c) and (e) shows the active and reactive power plots during the disturbance. Active power during the fault reduces corresponding to the PCC voltage dip with corresponding changes in reactive power without P/Q priority or fast fault current injection. Voltage support through reactive power can be provided with all PLL types even with weak grid scenario. Phase angle jump during the impedance change and fault can be observed but return to the pre-disturbance value after few cycles of oscillation and follows the trend of second dip in voltage which could trigger protection settings, if not taken care of in the recovery period.



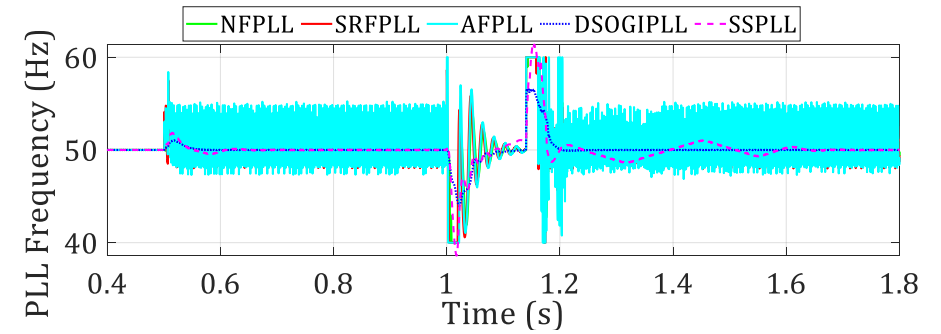
(a) Voltage at PCC



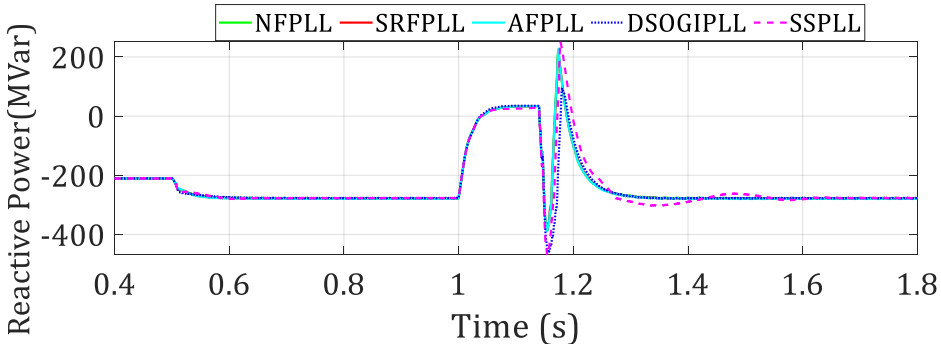
(b) Frequency at PCC



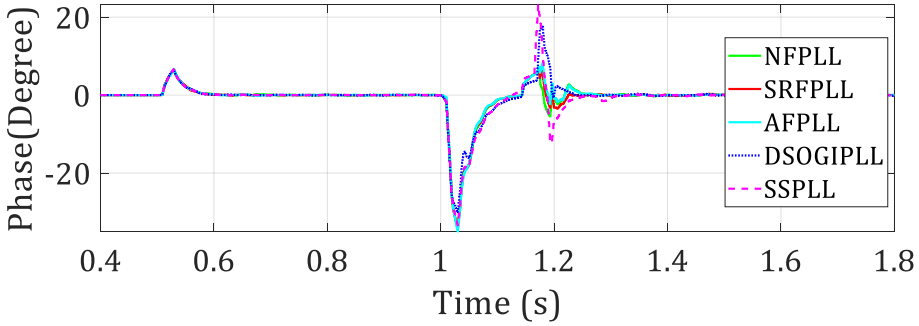
(c) Active Power Injected to Grid 1



(d) PLL frequency response



(e) Reactive Power response at Grid 1

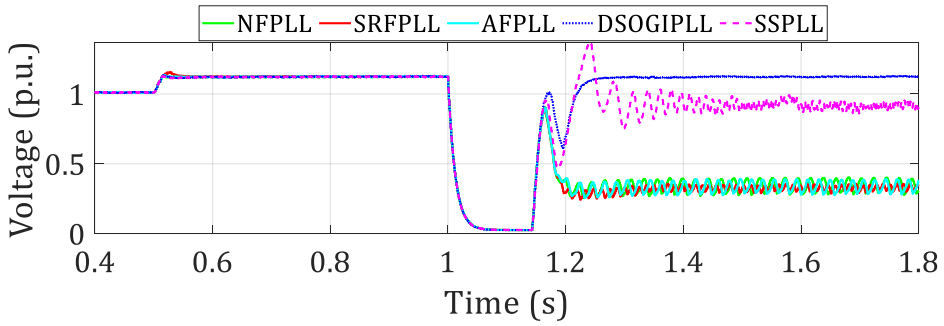


(f) Phase response at PCC

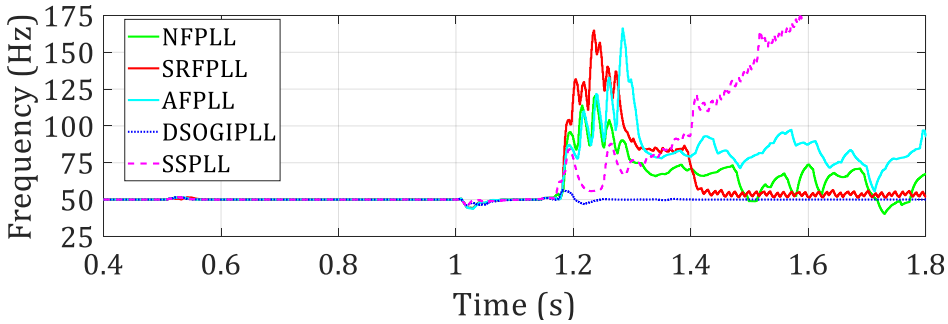
Figure 4 FRT Response for Weak Grid (SCR=3)

3.4 Case Study 4: FRT Performance of HVDC connection to very weak Grid with different PLL

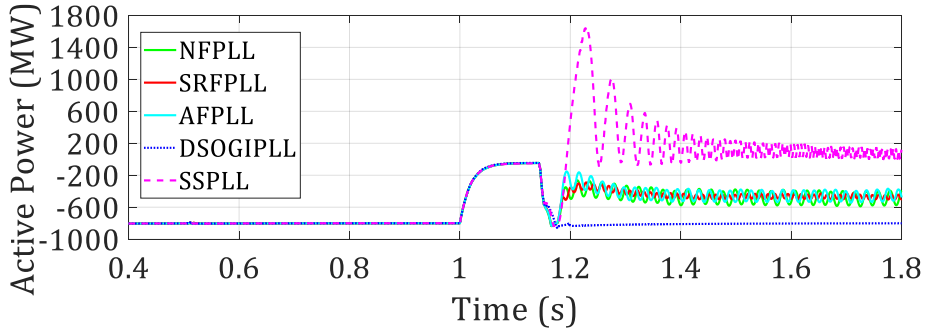
The performance of HVDC connection to very weak grid under severe fault with different PLL types is tested in this case. At *t= 0.5 s* the grid impedance is changed to emulate SCR=2 operation and at *t=1s* a three-phase symmetrical fault is applied at grid 1 for 140ms, as shown in Figure 5. Fault impedance is selected to retain 30% voltage at PCC during fault as previous case, however, can't retain the PCC voltage and thus the stability of the system is compromised, as shown in Figure 5(a). Only DSOGI based PLL tracks the frequency during fault while others hit the limits and oscillates from the steady state value causing instability. SS PLL recovers after the fault, but loses control following a second dip as shown in Figure 5(d).



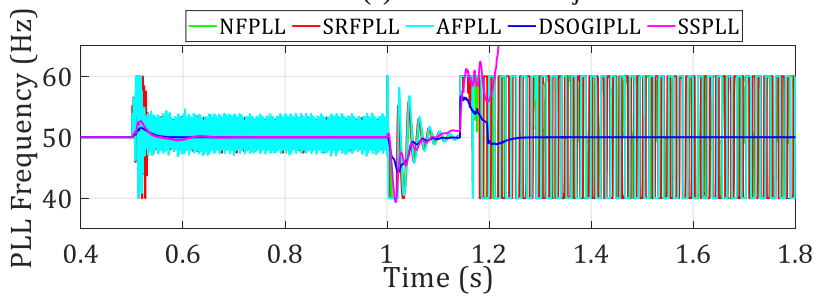
(a) Voltage at PCC



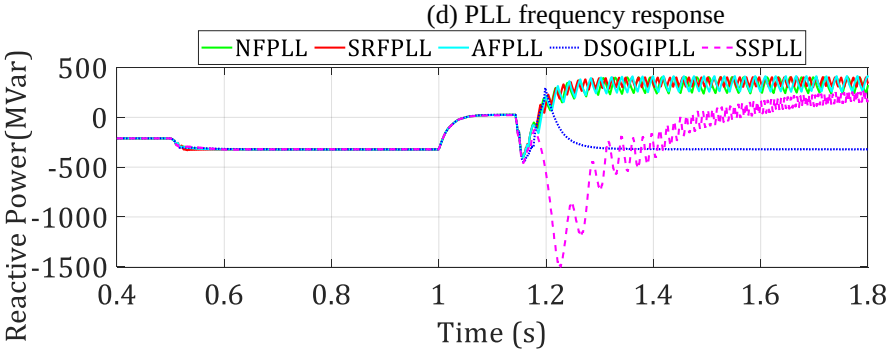
(b) Frequency at PCC



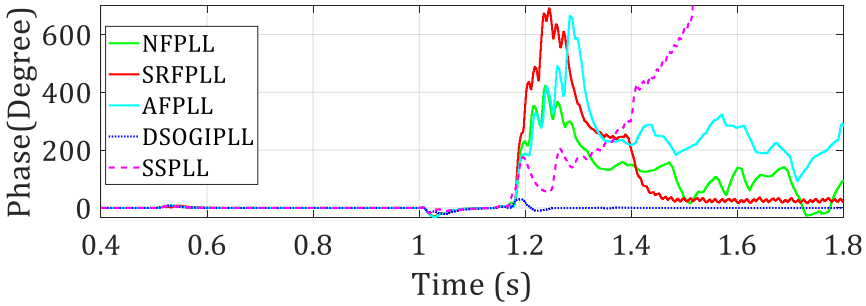
(c) Active Power Injected to Grid 1



(d) PLL frequency response



(e) Reactive Power response at Grid 1



(f) Phase response at PCC

Figure 5 FRT Response for Very Weak Grid

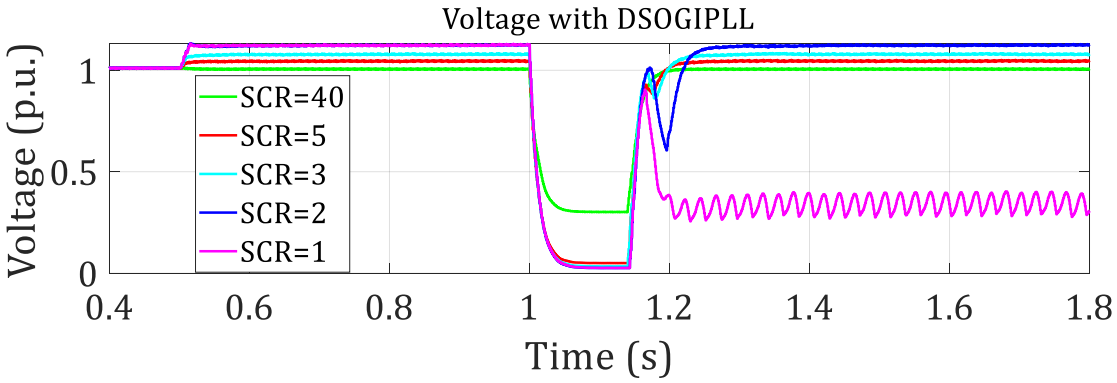
Active power during the fault reduces corresponding to the PCC voltage but recovers only when DSOGI PLL is used compared to other cases. As shown in Figure 5 (c) the inability of traditional synchronisation schemes in tracking voltage under very weak condition and when subjected to severe grid fault. No P/Q priority or fast fault current injection is considered which could improve the responses and is included in the grid code provisions to, however, aims only at strong girds. Voltage support through reactive power can be provided with only DSOGI, which is reflected by the instability in the reactive power as well (see Figure 5 (e)). Phase angle jump during the impedance change and fault can be observed in Figure 5(f) and is severe in all PLL types apart DSOGI. The cases study showcased the inability of traditional grid synchronisation schemes in providing stable grid connection of HVDC schemes and stress the need for their specification in Grid Code requirements

3.5 Case Study 5: FRT Performance of HVDC connection to varying grid strength with DSOGI PLL

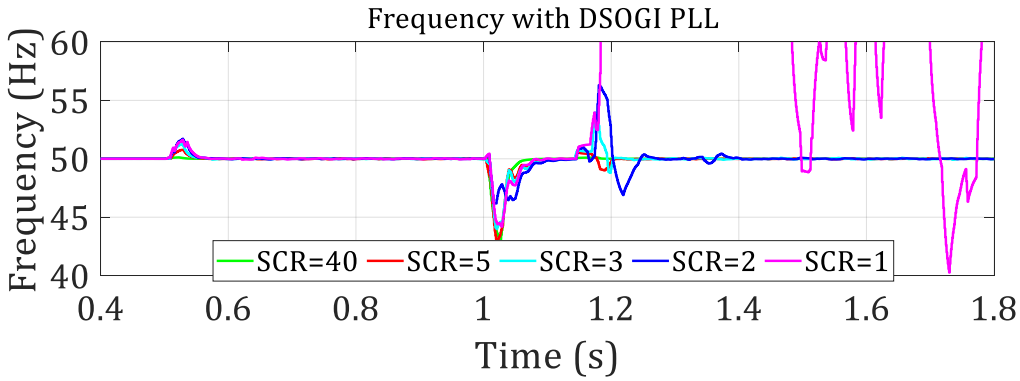
Previous sections identified the operational performance of HVDC connections when equipped with different PLL types and under severe grid faults. The conclusion drawn that DSOGI PLL delivers better transient performance for strong to very weak system (from SCR=40 to SCR=2) and outperforms all the traditional PLL types. To this end the operation of this type of PLL under extremely weak grid condition (SCR=1) is tested with the case study presented here.

The case is similar to previous sections and with DSOGI PLL is tested for very weak (SCR=1) operation. As shown is Figure 6 (a) the PCC voltage is stable until SCR=3, however, starts oscillating for SCR=1 with low frequency. Besides, the voltage drops down to the 0.3 p.u, and is therefore is below the Grid Code specifications. Thus, the voltage recovery is compromised even with robust DSOGI-PLL for extremely weak system operation The network frequency

also shows similar trend with SCR=1. Even though SCR=2 operation can be achieved with DSOGI extreme weak system operation is not possible and requires additional control modifications and tuning of the convertor controllers.



(a) Voltage at PCC



(b) Frequency at PCC

Figure 6FRT Response with DSOGI PLL for different SCR.

4 The Fault ride through studies for weak system: Impact of reactive current limit

In practice, the convertor capacity limit is further restricted by a current limit when operating under transient condition. When the reference current is saturated at its limit, the convertor behaves like a constant current source in which case the convertor power is limited by the rated capacity indicated by the maximum current limit. The Network Codes by ENTSO-E and NGESO has specified how convertors should provide “maximum” reactive current and “fast” fault current, but the terms maximum and fast are ambiguous and not defined explicitly [7-8]. This is significant for weak grid scenarios.

Requirements for active and reactive power recovery and protection settings is another aspect which requires careful consideration in a weak grid operation. Generally, under a close-up fault, Synchronous generator will instantly contribute a fault current at 5-7 pu. In the meantime,

a convertor can only provide a current of 1-2 pu or even lower than 1 pu under extreme conditions. In some cases, it seems that convertors shall produce fault current with a delay (during which there could be an initial dip) and then followed by a ramping up of current whose rate is not defined. The GB grid code states that the fault clearance times need not be less than 80 ms (typically ranging from 80 ms to 100 ms). With typical circuit breaker operation times of 50 ms , this means that faults shall be detected by the protection system in around 30 ms, although many relays can do this in 20 ms or less [8].

A procedure is set-up and demonstrated here using the test system shown in Figure 1 to determine the requirement of transient current for fulfilling the Grid Code requirements. This method investigates successful recovery using practical transient current ratings and reactive current limits for very weak system operation. The procedure is outlined below.

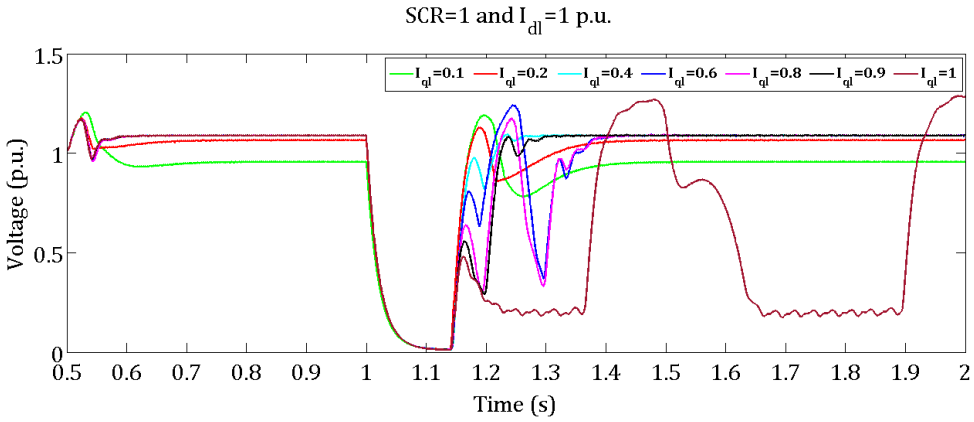
1. Begin with a typical VSC current limit of about 1.1pu.
2. Then, test a range of maximum reactive current contribution levels to determine if any of these conditions result in a successful recovery after a severe fault condition.
3. The reactive current contribution in this test was adjusted from 0.2 to 1.1pu.
4. Consider a 3ph-g fault at the inverter terminal to generate a worst-case fault condition.
5. Ensure that the system recovery satisfies the grid code requirements for the normal operation range as specified in GB Grid Code, that is between 49Hz and 51Hz.

The test procedure was applied to the test system described in Section 2. Figure 1 shows that regardless of the contribution of reactive current, having a total current rating of 1.1pu does not return the voltage to its pre-fault steady-state value. To confirm this and the contribution of PLL following cases were implemented and tested.

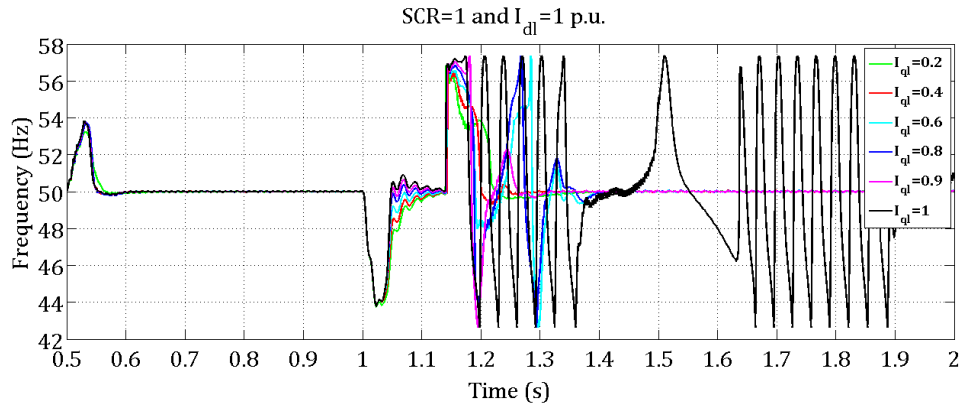
4.1 Case Study with DSOGI PLL

From Section 3 it is clear that DSOGI-PLL offers better transient performance. To evidence this for the case study presented here operation of HVDC link with DOSGI-PLL is considered for extremely weak grid operation. At $t= 0.5\ s$ the grid impedance is changed to emulate SCR=1 operation and at $t=1s$ a three-phase symmetrical fault is applied at AC grid 1 for 140ms as shown in Figure 7. Extreme weak grid operation with SCR=1 is considered with an active current limit set to 1 p.u. Varied the reactive current limit from 0.1 p.u to 1 p.u. to evaluate the operation of HVDC and its compliance with Grid Code requirements. Extreme weak grid operation is possible by carefully adjusting reactive current limit without changing the

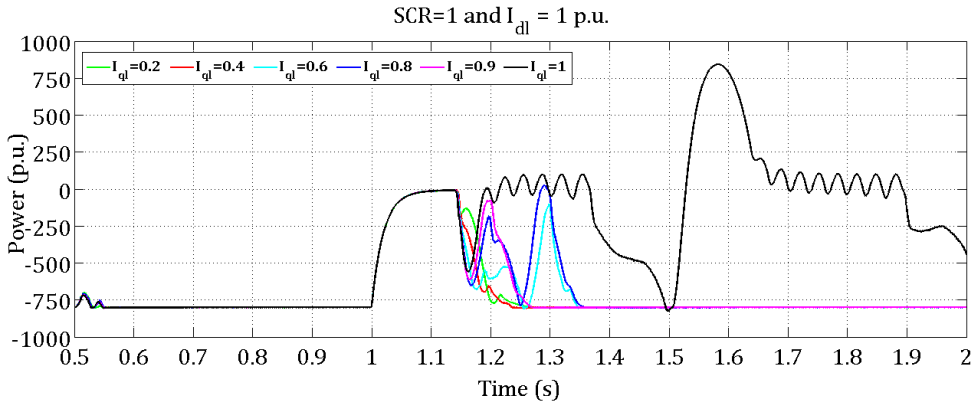
convertor control. However, the contribution of reactive current to post fault recovery is depend on the convertor transient current rating. This is also evidenced in Figure 7(a) that as long as the maximum reactive current limit is 0.9 p.u or below, the voltage recovery is acceptable.



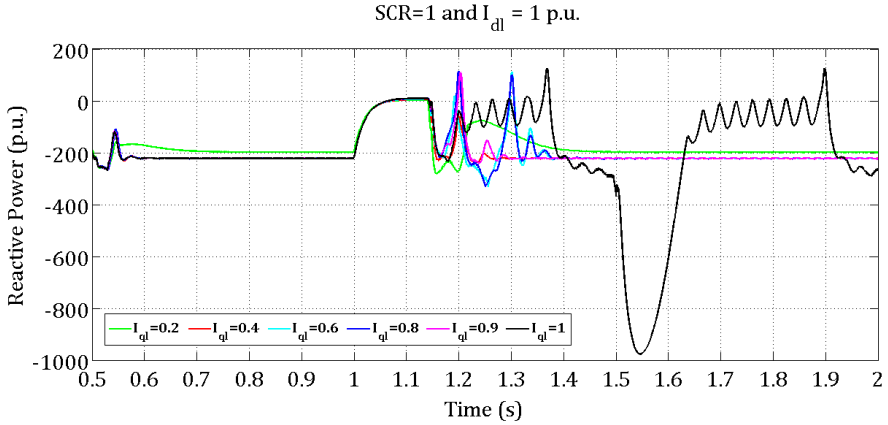
(a) Voltage at PCC



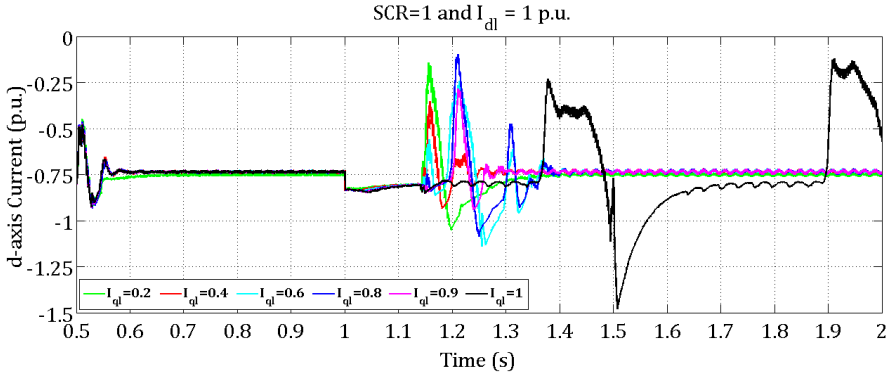
(b) Frequency at PCC



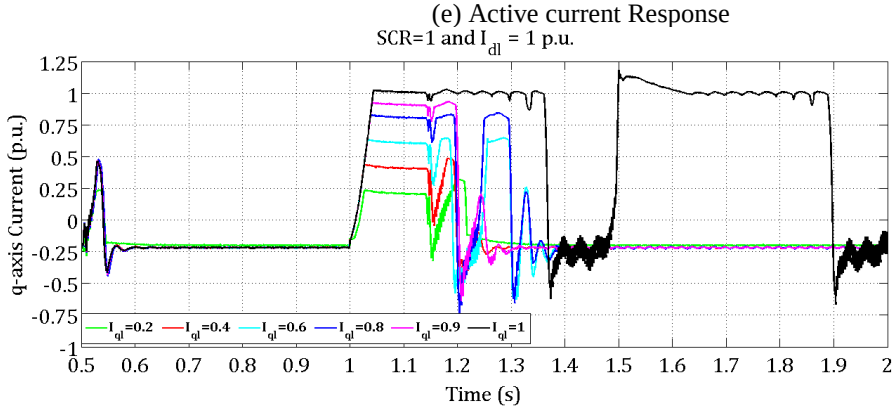
(c) Active Power Injected to Grid 1



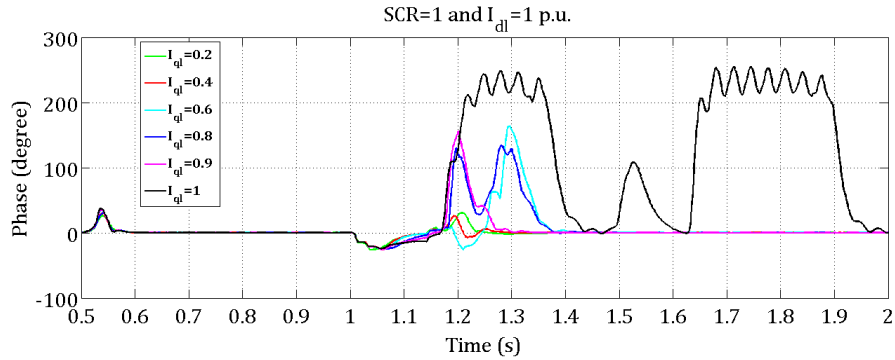
(d) Reactive Power response at Grid 1



(e) Active current Response



(f) Reactive current Response



(g) Phase angle response at PCC

Figure 7 Reponses with FRT subjected to different reactive current limits with DSOGI PLL

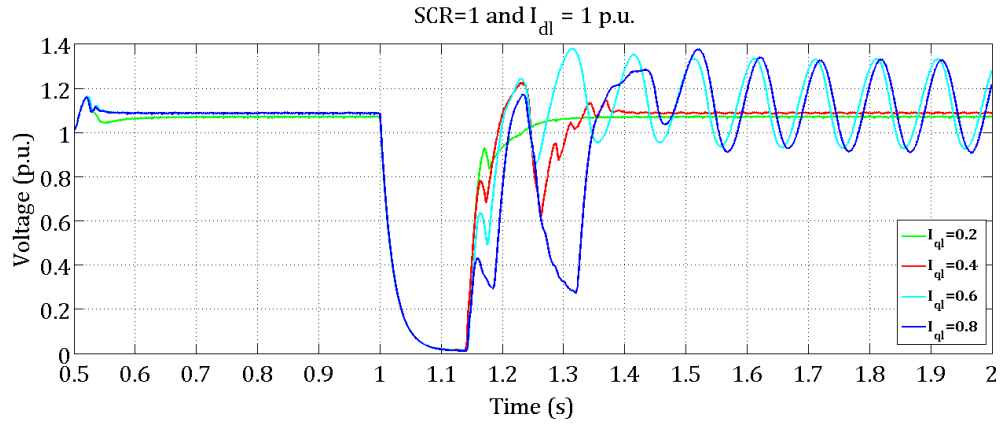
The active power order is set for 800 MW while the reactive power is set for -200 MVar. Very weak grid operation with SCR=1 with limited d-axis current produces zero active power during fault interval and returns to pre-fault disturbance state depending on the reactive power contributions. The reactive power follows similar trend with support provided during fault. The results showed that if the maximum reactive current limit is between 0.2 and 0.9pu the network can return to its pre-fault value.

The reactive and active current contributions during and after the fault are shown in Figure 7(e)-(f). The reactive current at the recovery is kept at the maximum and the remainder is used for the active current. This analysis concludes that the convertor current rating and the maximum reactive current limit determine the system recovery from the faults and these values need to be determined considering the worst-case system conditions.

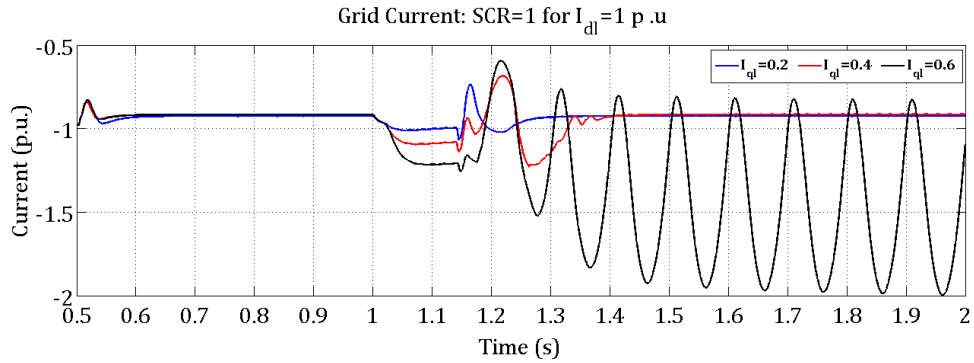
The VSC Inverter AC side frequency and phase response to a 3ph-g fault are shown in Figure 7(b) and (g). The frequency rides through the fault for all the cases, however, the post fault recovery is different for different reactive current limits. Operation under rated active and reactive power set-points are possible without much modification on the control systems as shown in Figure 7(c) and (d). However, pushing the reactive current limit without corresponding active current reduction will result in frequency and phase jumps, as depicted in Figure 7(g).

4.2 Case Study with SRF PLL

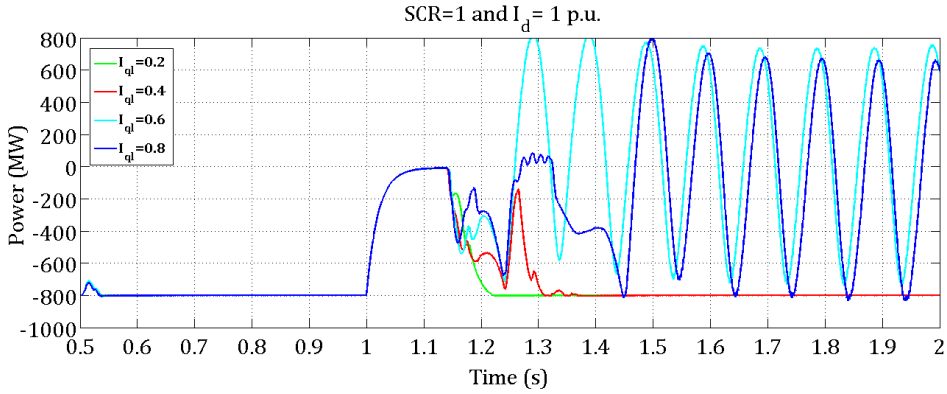
The standard vector control employed in HVDC connections uses SRF-PLL and is therefore considered in all the current Grid Codes. Thus, to identify its performance a case study is presented here. At $t= 0.5\ s$ the grid impedance is changed to emulate SCR=1 operation and at $t=1s$ a three-phase symmetrical fault is applied at AC grid 1 for 140ms. Extreme weak grid operation with SCR=1 and active current limit is set to 1 p.u is considered. Varied the reactive current limit from 0.1 p.u to 0.8 p.u. Extreme weak grid operation is possible by carefully adjusting reactive current limit without changing the convertor control but limited compared to DSOGI-PLL operation as shown in Figure 8. However, the contribution of reactive current to post fault recovery is depend on the convertor transient current rating with apparently only rated operation at 0.2 p.u is possible with SRF-PLL compared to 0-2 to 0.9 p.u operation with DSOGI-PLL. This is also evidenced in Figure 8(a) that as long as the maximum reactive current limit is 0.4 p.u or below, the voltage recovery is acceptable.



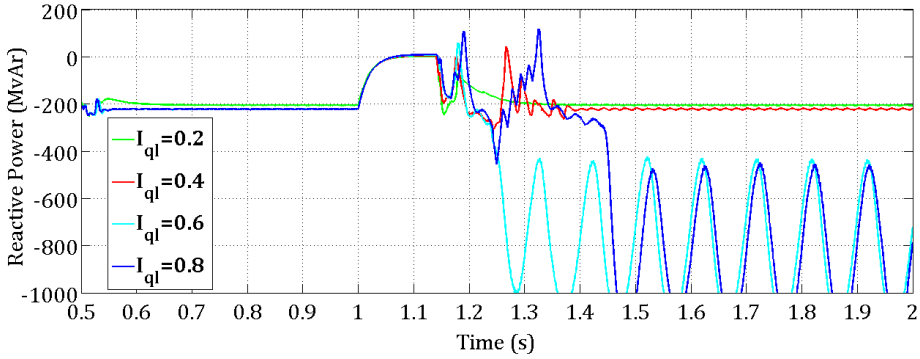
(a) Voltage at PCC



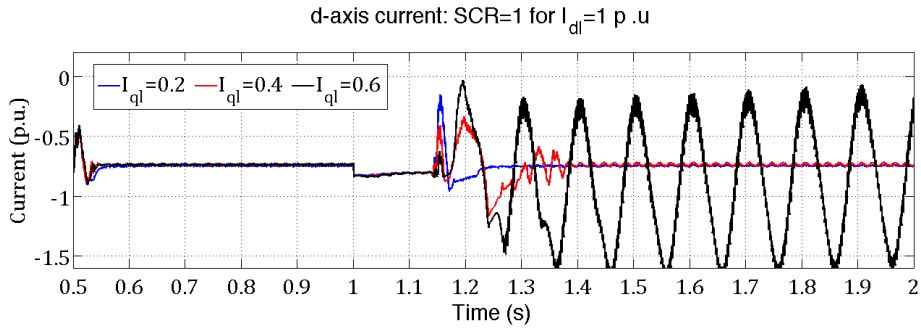
(b) The grid current response



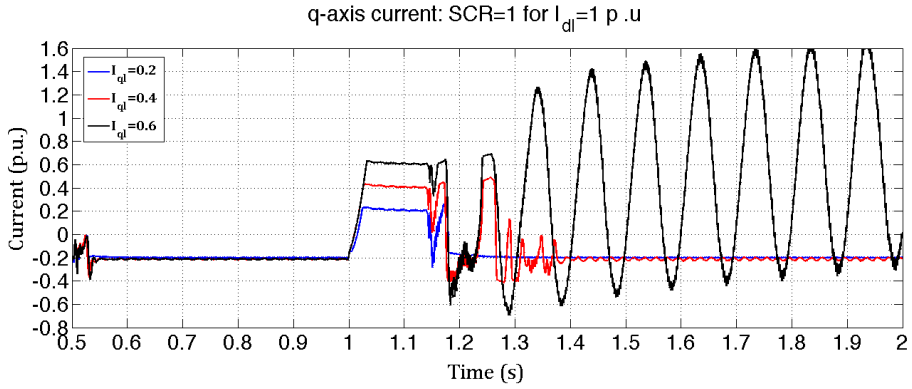
(c) Active Power Injected to Grid 1



(d) Reactive Power response at Grid 1



(e) Active current Response



(f) Reactive current Response

Figure 8 Reponses with FRT subjected to different reactive current limits with SRF PLL

The active power order is set for 800 MW while the reactive power is set for -200 MVar. Extreme weak grid operation with SCR=1 with limited d-axis current produces zero active power during fault interval and returns to pre-fault disturbance state depending on the reactive power contributions as shown in Figure 8(c). The reactive power follows similar trend with support provided during fault, depicted in Figure 8(d). The results showed that if the maximum reactive current limit is between 0.2 and 0.4 pu the network can return to its pre-fault value, however the oscillation takes few cycles to settle.

The reactive and active current contributions during and after the fault are shown in Figure 8(e)-(f). The reactive current at the recovery is kept at the maximum and the remainder is used for the active current. This analysis concludes that the convertor current rating and the maximum reactive current limit determine the system recovery from the faults and these values need to be determined considering the worst-case system conditions. SRF PLL based control is more sensitive to extreme weak grid operation compared to DSOGI PLL operation.

The grid current response during and after the fault are shown in Figure 8(b). The analysis concludes that the convertor current rating and the maximum reactive current limit determine

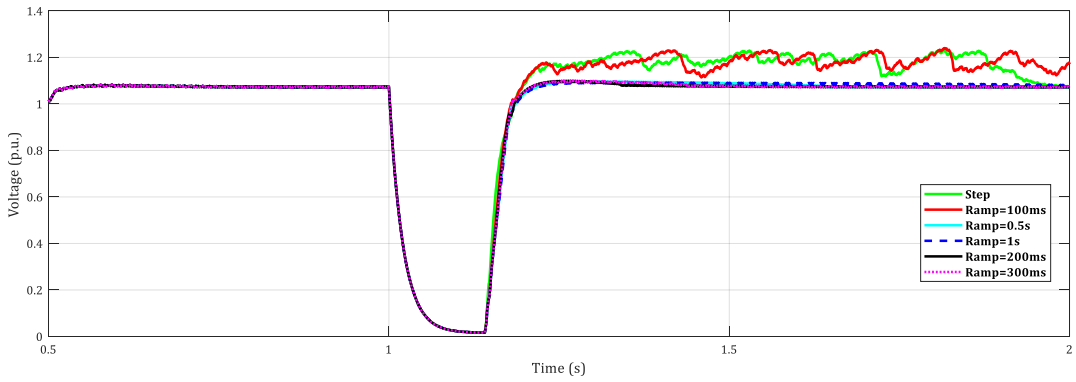
the system recovery from the faults and these values need to be determined considering the worst-case system conditions. The very weak grid operation is possible with SRF PLL if the active and reactive currents and within the total current limit. Note that this indicates that a certain amount of active current is necessary to support the recovery as well.

This analysis concludes that the convertor current rating and the maximum reactive current limit determine the system recovery from the faults and these values need to be determined considering the worst-case system conditions. For the test system used, a current rating of 1.1 pu and a maximum reactive current limit of 0.9 pu with DSOGI-PLL is suitable for extreme weak grid operation, if that is required in the future Grid Code specifications

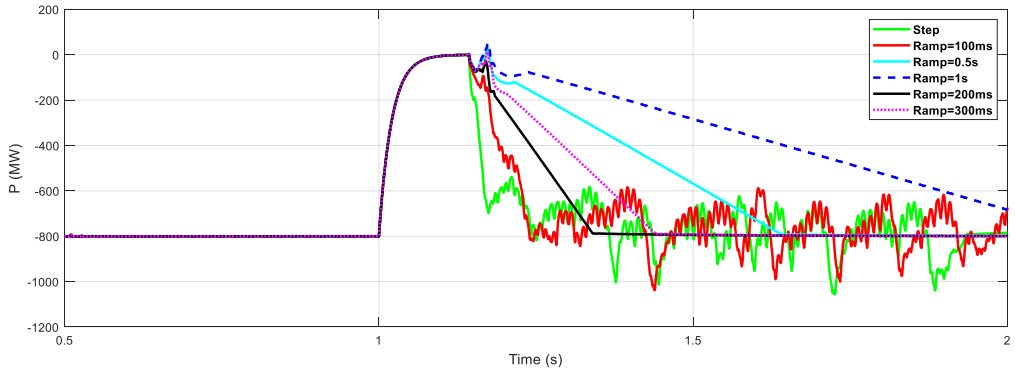
5 The Fault ride through studies for weak system: Impact of Ramp rates

The technical specifications in the current Grid Code on ramp rate limits after a fault is considered in this case study when the HVDC is connected to a very weak system.

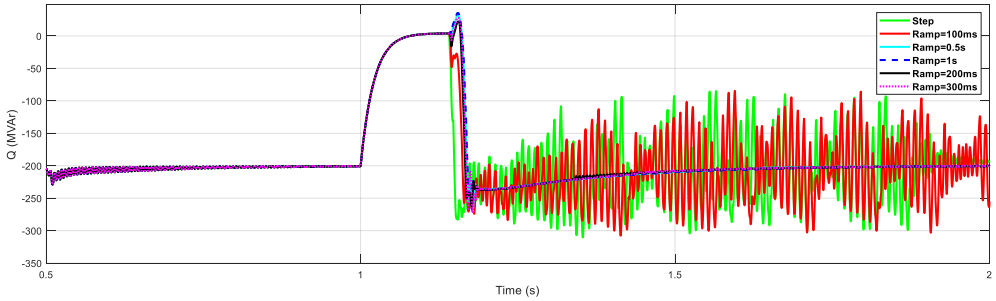
At *t= 0.5 s* the grid impedance is changed to emulate SCR=2 operation and at *t=1s* a three-phase symmetrical fault is applied at AC grid 1 for 140ms. The active current/power recovery rate after fault is varied to evaluate the performance of HVDC connections. Very weak grid operation is possible within the GC requirements by carefully setting the ramp recovery rate of Active Power 200 ms time provided in the current version is used as the reference and compared against PQ step change after fault recovery. The case study is performed on the test system depicted in Section 1 Figure 1.



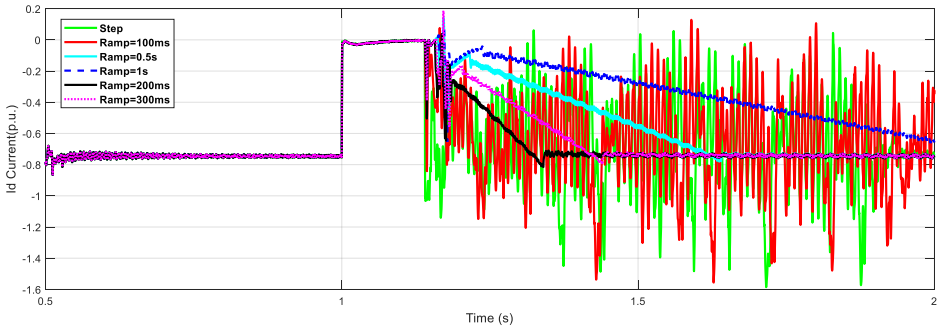
(a) Voltage at PCC



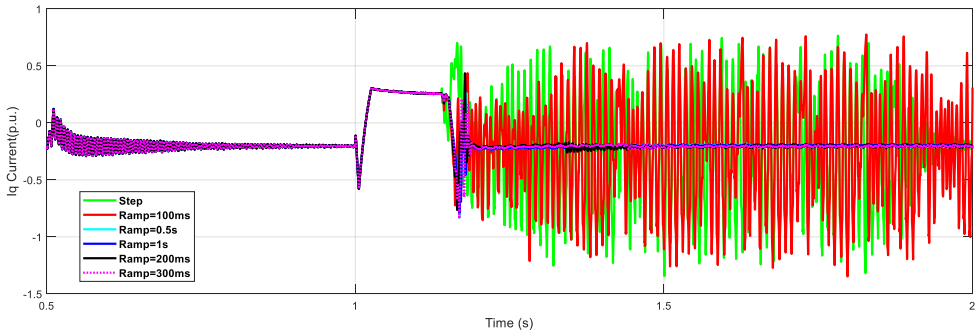
(b) Active Power Injected to Grid 1



(c) Reactive Power response at Grid 1



(d) Active current response at Grid 1



(e) Reactive current response at Grid 1

Figure 9 Reponses with FRT subjected to different ramp rates with DSOGI PLL

The system responses for step and ramp changes in the recovery of voltage s and power are shown in Figure. 9. As evidenced in Figure 9(a) that as long as the ramp rate is 200ms or above, the voltage recovery is acceptable for very weak system as well. This is also evidenced in the active and reactive power responses in Figure 9(b)-(c). The reactive and active current

contributions during and after the fault are shown in Figure 8(d)-(e). The reactive current at the recovery is kept at the rated value and the active current dictates the recovery rate.

From the case study it can be concluded that for very weak grid operation for with PQ control mode considering the following ramp rates

1. 100%/s = 100% in 1 s.
2. 200%/s = 100% in 0.5 s.
3. 1000%/s = 100% in 100 ms.
4. 100% in 200 ms.
5. 100% in 300 ms.

First three are part of Grid Codes with two and three are included in the GB code. Sufficient operational stability can be achieved with slower recovery rate allowing the voltage to recover and settle down to the pre-fault vale before the active power can be ramped back to the rated value. Besides, using step as a provision of ramping back the active power to the pre-fault value causes instability, since the voltage haven't reached its pre-fault value, causing control and synchronization issues.

6 Experimental Test and Analyis of Fault-ride through Requirments for Varying Grid Strength

For the analysis the AC grid is modelled in RSCAD/RTDS to represents different grid strength by varying the impedance. Steady-state and three-phase to ground fault cases were tested and demonstrated. For the test a voltage retained level of 50% is implemented with a three-phase fault scenario.

6.1 Experimental Set-up

A real-time hardware-in-the-loop experimental setup as shown in Figure. 10 is built to verify the simulation results concerning the SCR effect on the FRT requirements of HVDC connected to weak AC system. Real-time simulator based on RTDS/RSCAD platform has been used to emulate the weak AC grid condition of HVDC connected power system. The VSC is implemented as a two-level a symmetrical monopole configuration and the control algorithms are programmed in dSPACE DS1005. The dSPACE board performs data acquisition,

monitoring and control of each VSC. Digital and analogue signals are transmitted back and forth between the dSPACE and the VSC using a Simulink interface. A grid simulator serve as an interface between the RTDS and the VSC test-rig and is a four-quadrant power amplifier rated at 2 kVA and 270 V rms (line-to-ground). The amplifier absorbs power from VSC2 and injects it back to the mains supply. The GS receives a low voltage signal from the analogue output cards (GTAO) of the RTDS. With this, it produces a three-phase mains supply voltage of 140 V. This supply voltage is the input of the isolation transformer connected to VSC2 of the HVDC test-rig. Therefore, 140 V in the test-rig is equivalent to 400 kV in the RTDS. This is the forward path between the RTDS and VSC test-rig. Finally, a three-phase current measurement from the test-rig is fed back to the RTDS via its analogue input cards (GTAI). This closes the loop between the RTDS and the VSC test-rig.

The DC link contains the necessary components to form a dc network, including a scaled-down representation of dc cable circuits, a dc short circuit generator and an insulated-gate bipolar transistor (IGBT) controlled variable resistor. Different network topologies (dc link, radial or meshed MTDC grids) can be achieved through suitable connection of the dc cables by using additional resistors and dc inductors. The specifications and parameters of the VSC-HVDC test-rig and HiL platform are provided in Table 3. For more information about the experimental set-up connection details and device specifications can be found in [10].

Table 3 RT-HiL platform: specifications and parameters

Devices	***Specs***	***Rating***
Convertors	*Rated Power*	*1 kW*
	Rated AC Voltage	*140 V*
	Rated DC voltage	*250V*
	Topology	*Two-level, symmetrical monopole*
AC Inductors	L_{g1}, L_{g2}	*2.2 mH*
DC Capacitors	C_{g1}, C_{g2}	*1020μF*

DC line	*L_{dc}, R_{dc}*	*2.4 mH, 0.26 Ω*
VSC Control System	*dSPACE DS1005/ControlDesk 3.2 (Simulink interface)*	
Real-time Simulator	*RTDS/RSCAD, Racks: 2. Cards: 2 GTWIF, 4 PB5, (2 GTDI, 2 GTDO, 2 GTAI, 2 GTAO, 2 GTNET)*	
Control Modes	*VSC1: Vdc/Q; VSC2: P/Q*	

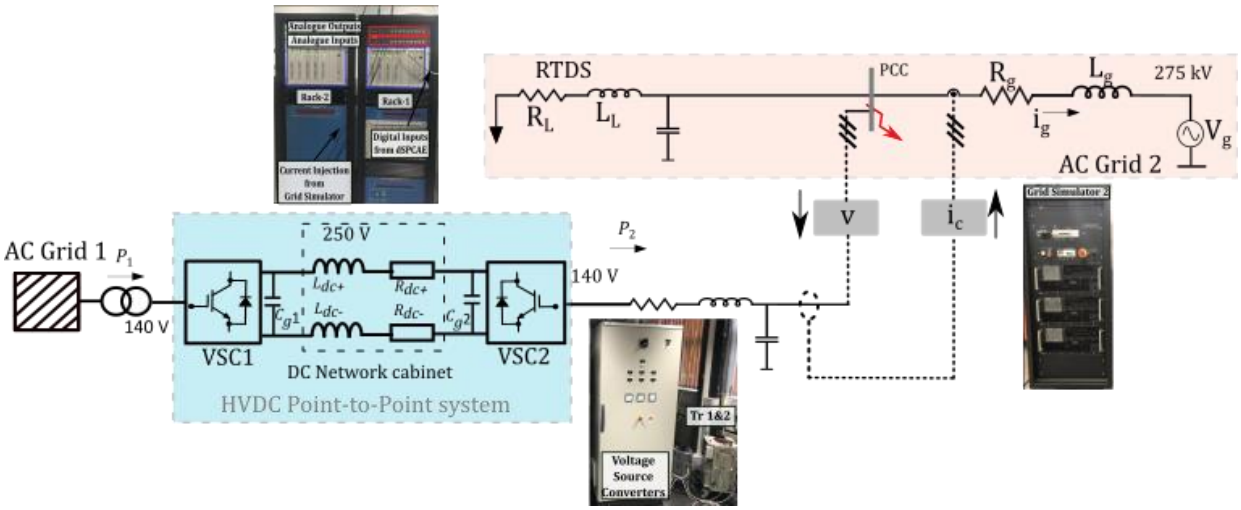


Figure 10 RT-HiL Configuration and Connection

6.2 Experimental Results

The RT-HiL experiments were performed for the set-up described in the previous section. The experiment starts with the system operating in steady-state and with strong AC grid connection. A three-phase fault (50% voltage dip) is emulated by the controlled impedance fault at the PCC inside the real-time simulator and cleared after 140 ms. The experimental results are plotted in Fig.12 and 13. The control modes of HVDC link are described in Table.3. The VSC 2 is first operated in normal operating condition with 1kW active power flow between the HVDC link and 0.2 kVA reactive injection into the grid. Two test scenarios were evaluated

(a) Cases Study 1 (CS1): Weak Grid connection of HVDC
(b) Case Study 2 (CS2): FRT of HVDC connected to grid with varying strength

For CS1, a weak grid operation is emulated by reducing the grid strength into marginal case (SCR=5) and injected P =1kW (I p.u.) into the AC grid as represented as a current change as in Figure 11. With such a large power injected from the HVDC into the grid when operating at a marginal case, instabilities in AC systems voltage and current can be observed. This indicates the connection challenges for a steady-state operation, indicating HVDC weakens grid operating at low SCR level. In other words, HVDC connection causes the impedance of the AC network to further increase thereby reducing the overall grid strength. At this stage a further small disturbance can compromises the system stability

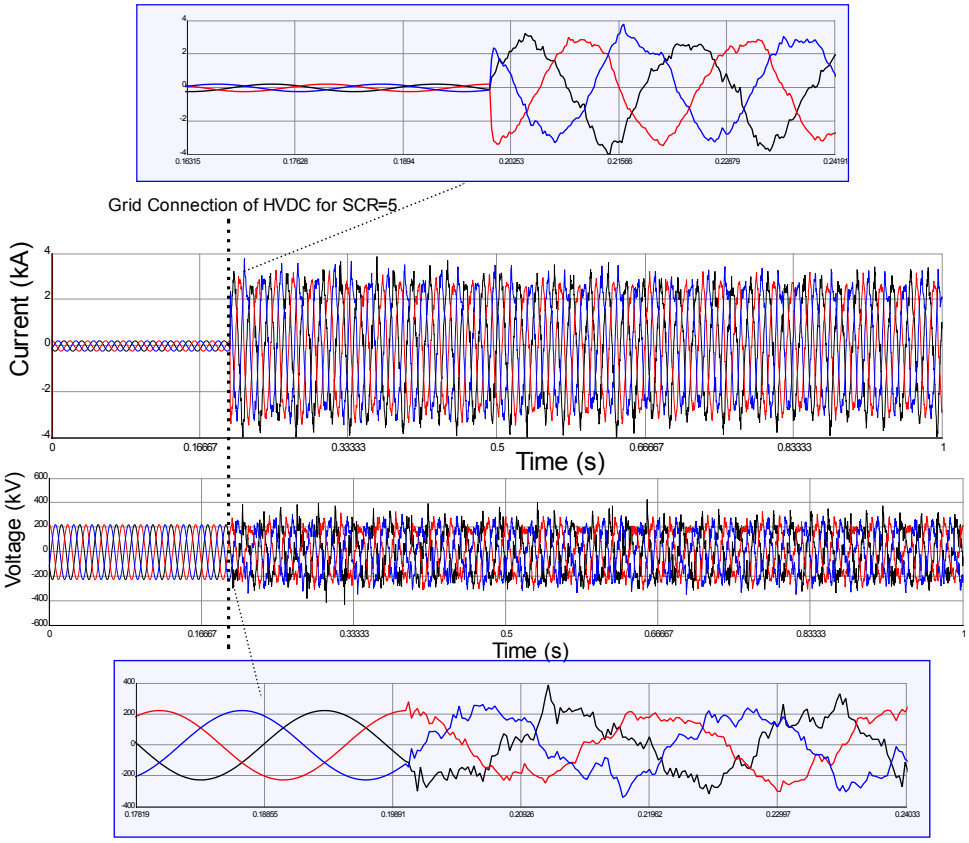


Figure 11 Weak Grid Connection of HVDC and netwrok paramters

For CS2, three operating conditions were evaluated during FRT operation; Strong (SCR=40), Marginal (SCR=5) and Unstable (SCR=2). A three-phase to ground fault is initiated and cleared after 140 ms. During the fault the grid voltage in *dq* frame and power injection from the HVDC to the AC grid is monitored and evaluated as in Figure. 12. Where *dq*-axis voltages are shown in red and blue colour respectively with active power injection from HVDC is shown as green colour.

For the stable case as in Figure 12(a) fast fault recovery is attained and the voltage dip is as expected (50%). The recovery rate is within ms and thus active power delivery can be achieved after the fault. Similar trend exists for marginal case as well (see Figure 12(b)), however, as the grid strength reduced the voltage dup is further compared to the stable case during a severe three-phase fault.

As depicted in Figure 12(c), on the other hand, with reduced system strength, less active power delivery in the weak grid (SCR=2) will not only threaten the stability but also worsen the voltage recovery rate. Additionally, extra consumption of reactive power from the grid during the fault condition will hinder the voltage recovery following the fault clearance. This is evidenced by the increase in q-axis voltage component in Figure. 12(c), depicted in red.

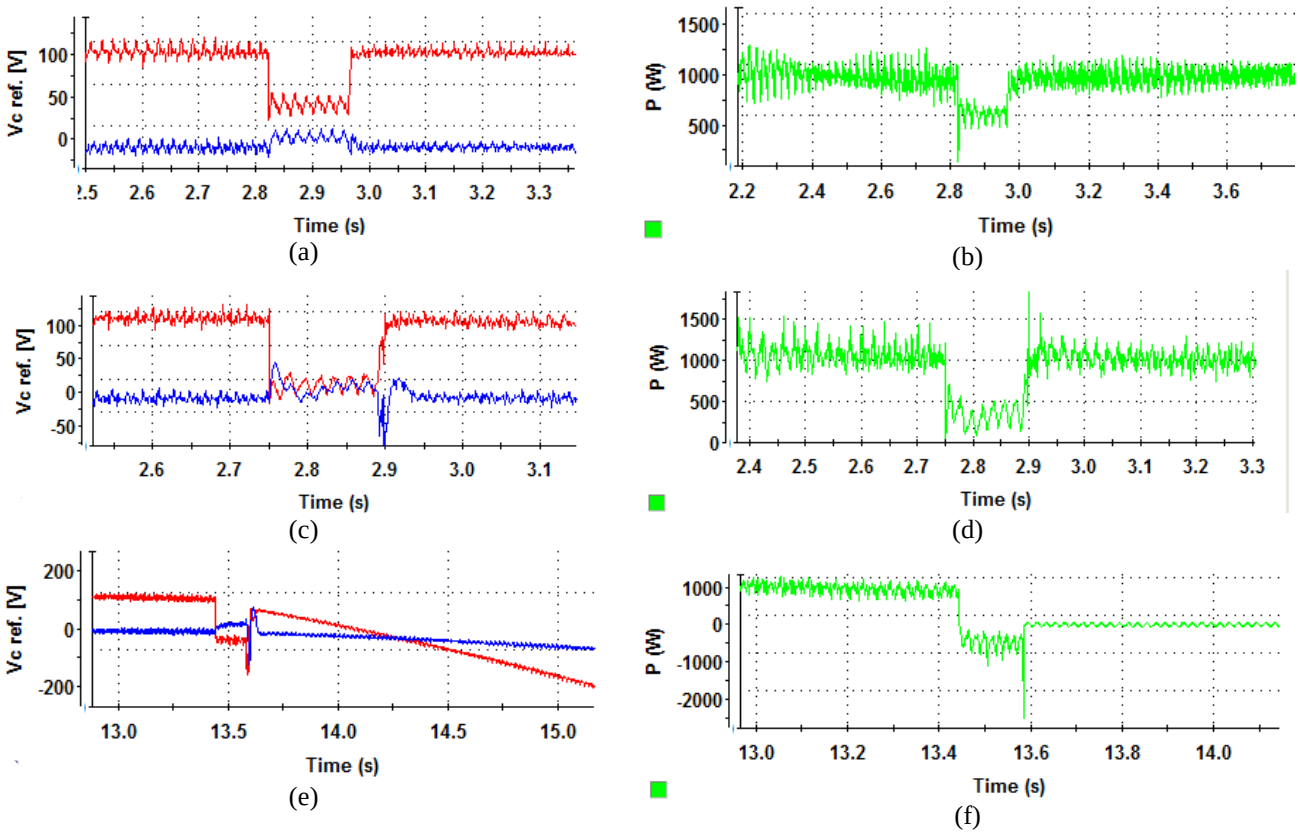


Figure 12 FRT response of HVDC connected to AC grid with varying grid strenghth for three cases

7 Potential specification of requirements: Remarks and Recommendations

From the review, analysis and case studies performed the challenges of connecting HVDC schemes and compliance with the existing GC for weak grid scenarios can be summarized as:

1) Utilization and Complexity of PLL models: According to the literature, the most commonly used PLL model is the SRF-PLL. Despite being a standard, the model is not robust enough to

operate under weak grid conditions. However, DSOGI-PLL is less common and among all considered models but outperforms all other types, the SS-PLL, in fact, is the most complex as it requires to introduce a additional filters to work properly. Models AF-PLL and NF-PLL, on the other hand, are the simplest models, however, inferior in operation compared to DSOGI-PLL.

2) Dynamic Performance: For severe disturbances, e.g., three-phase to ground fault, all PLL models show very similar transient response until weak grid operation, that is until SCR=3, even if they saturate. On the other hand, significant differences of the dynamic response of the PLL models are observed for very weak (SCR=2) and extremely weak grid (SCR=1) operation. In these cases, the dynamic response of the DSOGI-PLL model is the best choice as it locks the PI internal state variable and reduce the delay of the operation of the controller when the input signal is back to normal.

3) *Recovery rates and current limits:* Compared to the existing requirements on reactive current limits, careful consideration is required for operating the HVDC links in very weak and extremely weak system conditions. This is also identified for PLL types with DSOGI-PLL a wide operating range is possible 0.2 p.u.-0.9 p.u, compared to 0.2-0.4 p.u. with SRF-PLL which is significant when designing fast fault current injection schemes for voltage support.

On the other hand recovery rate as identified in the current Grid Code will suffice the need for weak-grid operation ass identified through this study.

4) Best Practice: For the compliance of HVDC connections to weak and very weak real-world power system networks under severe transient cases, the best practice is to carefully model PLL controllers with respect to the gird strength. Besides, selection of associated control system parameters according to the actual hardware and specifications provided by the vendors of the VSC devices is recommended. If the real implementation is unknown, the choice becomes a trade-off between dynamic performance and implementation complexity should be accounted for. Whenever priority is the performance following a large disturbance, DSOGI-PLL is recommended for weak grid operation. On the other hand, when active power recovery is the priority a recovery rate of 100% in 200 ms, is recommended.

8 Conclusions

The GB Grid Code does not demonstrate a min/max SCR at the PCC during Fault Ride Through and normal operation which will change across operation and connection of new convertors. Although different PLL choices and their tuning influence the performance and resilience of the convertor- however it is not clear in current GC data exchange what choices are being made and what consequences these have. Transients such as three-phase to ground fault is more severe with weak grid operation, however, other faults are more challenging still- and data exchange of models for this not currently supported within Grid code. In addition, it is not clear how the technical issues related to tracking of convertor operation under different control modes is required to be modelled Besides, stages of convertor operation; pre-fault, during and post-fault is not identified and/or needs to be considered for weak grid connection in the Grid Codes.

In addition, from the range of analysis performed, several other points can be concluded that de-loading a convertor helps its stability during FRT and also in recovery, lower SCL drives slower power recovery, the choice of PLL is critical both for steady-state and in particular for transient response, as is how FFCI is delivered. Moreover, no perfect tuning of control exists across high and low strength conditions, even when convertor rides though it takes a long time to settle down under weak grid operating conditions. To this end it should be noted that the things that influence these areas of performance are not part of current grid code data exchange.

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