HVDC challenges in meeting current GB Grid Code in a weak network

The National HVDC Centre

Purpose

This document is a summary of the questions, answers and discussions from the webcast co-hosted with the Cardiff University on Friday 20 March 2020.

Reference Document:

Presentation slides available: https://www.hvdccentre.com/wp-content/uploads/2020/03/HVDC-Grid-Code-Challenges_Cardiff_200320_v1.0.pdf

If you have any further questions, please email us at the link below.

Questions and Answers

Q1: Does this analysis apply to both Current Source Converter (CSC) and Voltage Source Converter (VSC)?

A1: Yes. The analysis focusses on VSC HVDC however many of the challenges around FRT- which was found to be the most severe of existing GC tests are challenges for LCC also.

Q2: SCR is no longer a useful parameter on its own. What do you mean by Short Circuit Ratio (SCR) and Short Circuit Level (SCL)? You need to discriminate between STIFFNESS (defined by # and rating of grid forming devices) and FAULT CURRENT that can flow. STIFFNESS and FAULT CURRENT can be quite different in converter-dominated grids.

A2: Agreed; however in the current scope of Grid code data the information on the extent of convertor infeed contribution locally within a network model is not available, Cardiff University have therefore considered the simple network model to define strength- you are quite correct that the actual behaviour for a given SCR in an actual network could prove more severe.

Q3: What is a typical Fault Ride Through requirement for the timing of active power restoration after a fault is cleared?

A3: That's a Classic "it depends" question. The lower the network strength, the harder the tracking, the greater reactive current is reserved for maintaining convertor stabilisation. the speed of stabilisation in a real system involves more than just the individual convertor being considered here and the damping time will be different in different areas of the system based on their characteristics and those of the connected convertors.

Q4: Different manufacturers utilize different converter control under transient conditions i.e. ac grid fault, consequently the converter at PCC may have different behaviour. The proposed solution to limit the active power (P) under recovery can not be used as general approach.

A4: Quite agree- and could be dangerous to rate of change of frequency (RoCoF) for example if all convertors were doing it in response to a common voltage depression during a fault- as you say different manufacturers have different control strategies and options around this- and different network areas will have different priorities over how they need to recover- we need to get the best balance. Power de-loading is just an illustration of one approach.

Q5: My experience is that vendors hold their PLL designs very close to their chest. Is the general PLL type known for each new HVDC link?

A5: Exactly right- this is a challenge at present- we cannot see what's "under the hood" and are infering it- this and other analysis is seeking to highlight what areas of control structure require greater openness to improve their integration- or accuracy in modelling however flattened models being exchanged may be.

Q6: DSOGI PLL is that a trade name?

A6: Double second order generalised integrator. More info is in the National Grid ESO project report and other literature on this shown on Page 20 of the slide deck. Here is another referece. M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase pll structure based on second order generalized integrator," in Power Electronics Specialists Conference, 37, pp. 1–6, 2006.

Q7: When the fault occurs, are you intercepting the Phase Lock Loops (PLL) and taking alternative action? Most industrial PLLs go into a "dead reconing" mode when a fault is detected. You pull back the angle and frequency from some time (you hope) before the event and then dead-reckon until the fault goes away. This is my understanding of how most manufacturers will operate their converters. Is this included in the PLL analysis?

A7: The detail of the PLL is in the report mentioned above on Page 20 of slide pack - but you are correct- based on measurement tolerances they will enter states of being unable to track. The tolerances for this and criteria for coming out of this dead state can equally influence convertor stability and any mis-tracking during the fault or immediately after could spark a contagion impact on the tracking of other PLLs near their limits. Hope that helps.

Q8: Did you test DDSRF-PLL for this analysis ?

A8: A generic SRF -PLL was used- we recognise many PLL approaches exist those of focus were informed by the earlier NGESO work identifying most likely and common forms on the GB system.

Q9: Very interesting work. Did you also study the voltage overshoot with different SCL?

A9: Voltage overshoot was observed in the study (see AC voltage curves on Pages 14, 17, 21, 27 & 29 on slide pack) but the extent to which this phenomenon was analysed is limited as this was not the major focus of the project.

Q10: Do you mean transformer's K factor?

A10: No. The k factor refers to the proportionate gain of the Fast Fault Current Injection (FFCI) control loop (an outer control loop)

Q11: Which software do you use when analysing HVDC system?

A11: Offline- PSCAD; experimental we are using physical two-level convertor hardware, which the PSCAD model has been constructed to represent.

Q12: How do you control voltage on the dc bus for the converter which has P-Q control? with dc capacitors?

A12: The DC voltage control is achieved using the traditional double current control in stationery dq-reference frame using the capacitors of the MMC convertors to balance and maintain the DC voltage

Q13**: SCR=5 is strong grid or weak? as I know SCR=3 and more is for strong grids**

A13: The experimental study considered SCR=40 as strong case; SCR=5 as marginal case and SCR=2 as weak grid case as shown on Page 36 of the slide pack.

Interactive Discussions with Audience

1. **How do you define system stiffness, in reference to the earlier question? Are there any defined methods? And if you ASSUME SCR 5.0 just accounting for your local impedance to the supergrid, then you may be actually at SCR=2 if the supergrid is actually consisting of a high ratio of current-loop converters. This is why SCR is so dangerous to consider as a main parameter. You NEED to know the grid stiffness, accounting for all connected generators and impedances. Just considering local impedance to some assumed infinite bus is no longer appropriate.**

A. Again we agree with this observation. One of the challenges for defining system stiffness is that many measures exist (and are being developed) across many TSOs and other institutions to describe system strength in a convertor dominated environment. As is described in our slides each definition has strengths and weaknesses for differing applications in analysis. There is no one definition at present that has been found to be equally good in all applications. We agree that a weakness of a lack of nearby dynamic modelling of the network could lead convertor infeed to be added to synchronous strength to provide a misleading view of system strength. Equally what "near" is in the context of a convertor-dominated network needs to be considered very carefully; the output of our previous webinar in describing small signal techniques to define regions of potential interaction allows for the areas requiring more detailed description to be better described to inform this question. This is a valid point and to study such detailed level of convertor grid interactions more information of the networks and associated components needs to be made available. This is one of our recommendations, to make available not just black box models, but detailed models to facilitate grid code studies.

2. **My question is it looks like some studies have been done with VSM. Am I correct that even in assuming that VSM has been used we are not getting a converged solution at SCR's or 1.0 or below. If this is the case how much tweaking was done to the VSM model.**

A. Our analysis has considered current approaches to control for convertors- these involve current-loop controls describing responses to near instantaneous grid measurements, and are as such very different to the concept of Virtual Synchronous Machines as is being codified within Grid Code modification GC0137 at present. Virtual Synchronous Machines function by having a defined phase relationship with the system as defined by an oscillator of the voltage source and associated controls related to defining inertia and an impedance between the voltage source and the point of common coupling. These controllers during faults respond inherently as defined by the impedance and inertia of the control, to an extent defined by the convertors rating and stored energy capabilities. Whilst current loops do exist in such control concepts, and would have PLLs associated with them, the ability of these to track the system voltage is not relevant to the VSMs transient behaviour. VSMs perform more like synchronous machines, with these secondary current loops relevant to the control concept performing a role similar to the PSS and static AVR of a synchronous machine control concept. As such VSM present similar traditional synchronous machine stability considerations, which at low SCL will present challenges but are defined and considered via current Grid codes. Further examination of VSM is an area for consideration which the project has identified as being an area of value.

3. **Any insight on how these conclusions could be applied to all inverter interfaced resources connecting to the grid, not just a large HVDC link?.**

A. The basic current loop control philosophy of VSC-HVDC is one common across all invertor control, albeit the specific structures tuning and application of such loops may differ in specifics. Equally the challenges surrounding the nature of black-boxed controls, their structure, their tuning and their applicability to wider operational conditions than defined within the current connection and compliance process are shared considerations. As we note across a series of Grid code modifications there are processes now underway to review and modify the grid code in this area.

4. **How do you define onshore and offshore hvdc connections, by their controllability?**

A. Offshore AC networks connected to HVDC have very different control philosophies as a result of their limited/ zero inertia and similarly low short circuit contributions. In order to support this the offshore HVDC control tends to be very different. It is likely to evolve further as it is applied to the context of the GB system. The subject is extensive and subject to development. The National HVDC centre has published a number of documents in this area {ref weblinks}and is currently across the Offshore Wind Industry Council, TOs and ESO providing input into the future direction of offshore development.

5. **Can you tell me OPEX value for submarine cables? what value do you use as a rule in percents? 1-1,5%?.**

A. This was not a focus of our work which was focused on aspects of grid code process rather than the operation and maintenance of the development.

6. **In case of VSC HVDC, do we have voltage or current control Loop for converter side?.**

A. Yes, both current control loop and the outer control loop were used for the VSC HVDC link.

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