# Strathclyde Engagement with the National HVDC Centre: Phase I Converter and GB Network Modelling

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**Executive summary**

This report presents detailed comparison of various offline and real-time user-defined models of full-bridge (FB) and hybrid modular multilevel converters (MMCs), with regard to the Switching function, Thevenin equivalent, and Averaged models. The user-defined real-time and offline simulation models employed in this report are developed in RTDS/RSCAD and PSCAD/EMTDC underpinned by theoretical basis described in the previous report\(^1\). Synthesis of different models of FB and hybrid MMCs is explained. For the purpose of validation, these models are compared extensively using identical parameters and controllers, and tested under a range of identical operating conditions, including AC and DC network faults. From detailed corroboration presented in this report, it has shown that the real-time averaged and switching function models of the full-bridge and hybrid modular multilevel converters produce near identical results as the respective offline switching function, Thevenin equivalent and averaged models of the FB and hybrid MMC. The study also highlights the enhanced control and operation of the FB and hybrid MMCs when compared to half-bridge MMC during DC faults. The developed models are well suited for further studies to fully explore the potential impact on system operation for FB and hybrid MMCs based HVDC systems.

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\(^1\) TR on Modular Multilevel Voltage Source Converter: Fundamentals and Synthesis of Different Models, Strathclyde-The National HVDC Centre collaborative research project, TR ref. USTRATH-HVDC Centre-P1-001, April 2018.
1 Introduction

In the last decade, a number of multilevel voltage source converters have been proposed for HVDC applications, with the half-bridge (HB) and full-bridge (FB) modular multilevel converters (MMC) taking the centre stage as the preferred topologies for multi-terminal HVDC grids. In the meantime, several hybrid converters were proposed as alternatives that offer an important trade-off between footprint, semiconductor loss, resiliency to AC and DC network faults and control range. Some of these hybrid converters are becoming increasingly attractive as they offer bespoke features, ranging from that of the HB-MMC to that of the FB-MMC.

Although the construction of large-scale DC grids using different converter topologies is important from both practical and market point of view, particularly for prevention of monopoly over supply chains, ensuring safe and reliable operation of DC grids with such diversity, present significant technical challenges; especially, during fault conditions.

Meaningful assessments of the interoperability of such complex DC grids require converter models with steady-state and transient behaviours that accurately resemble the typical behaviours of physical systems. All converter terminals (regardless of their topologies) must be designed to ensure that their steady-state and transient responses are confined within the narrow band with defined settling and rise times, maximum overshoots and permissible oscillation and damping in order to avoid undesirable interactions between converters.

With regard to modelling, concerted efforts from academia and industry in the last decade have resulted in the development of universal modelling frameworks for MMC and hybrid converters, namely, Thevenin equivalent model which was initially developed by Dommel in [1-4] and then extended to MMC in [5, 6], generalized switching function model [7-9], and averaged model [10-16]. Detailed studies presented in [6, 9, 17-21] confirm that all the aforementioned models are capable of reproducing the typical behaviours of modular and hybrid converters during normal operation, and AC and DC faults.

Equally, the control of MMC and hybrid converters is extensively investigated in the last decade [22-30]. There are two common methods for controlling MMC and hybrid converters. The first method only manipulates the phase and magnitude of the AC component for each phase-leg relative to that of AC grid as that in the two-level converter, with the DC components of the phase-legs fixed according to the desired DC link voltage. The second method manipulates both AC and DC components of each phase leg to control active and reactive powers, and to decouple capacitor voltage regulation dynamics from that of the DC link voltage.

The second control method allows the HB-MMC to control its DC link voltage independent of the submodule (SM) capacitor voltages, and vary its DC link voltage and retain control as long as the DC voltage remains above the peak-to-peak of the desired phase voltage generated by the converter. This method permits FB-MMC to offer maximum control range in addition to DC fault blocking, i.e., controlled operation over a wide range of positive and negative DC link voltages. Similarly, besides the DC fault
blocking, hybrid MMC with 50% FB SMs and 50% HB SMs offers controlled operation with zero to rated positive DC link voltage range.

As a follow up of the previous reports that have presented extensive offline and real-time validations of the HB-MMC models [31, 32], this report presents user-defined offline and real-time FB and hybrid MMC models which can be used for DC grid and system level studies. Both offline and real-time models employed in this report use identical controllers and parameters. The presented offline and real-time simulation waveforms show that the developed FB and hybrid MMC models are able to reproduce the expected behaviours during normal operation and AC and DC network faults.

2 Modelling and Control of Full-bridge and Hybrid MMCs

2.1 Modelling

Fig. 1 shows a generic power circuit of a three-phase MMC converter that consists of six arms, with each arm comprising of an inductor and a stack of HB or FB SMs, or combination of the HB and FB SMs as displayed on Fig. 2. Regardless of the types of the SMs, each arm of the MMC in Fig. 1 must be capable of blocking the rated pole-to-pole DC voltage. Complementary operation of the arms that constitute the same phase-leg is necessary to ensure that each phase-leg inserts appropriate number of SM capacitors (from the upper and lower arms) into the power path in order to build-up the needed instantaneous common-mode voltage to counter the DC link voltage, while allowing DC current to flow in a controlled manner. It is worth recalling that each MMC phase leg contains 2N SMs, but only N SMs could be selected for insertion into the power path, and the remaining 2N-N must be bypassed. The exact number of SMs could be inserted into power path depends on several factors such as the designed rated voltage per SM, and the type of SMs being employed in each MMC arm (HB, FB etc.)([31, 32]). Fig. 2 shows the generic phase legs of the HB and FB MMCs and of the hybrid MMC.

Fig. 1: Basic circuit of the three-phase modular multilevel converter
The upper and lower arm voltages ($V_{armU}$ and $V_{armL}$) for one phase of the generic MMC in Fig. 1 can be approximated as:

$$V_{armU} \approx \frac{1}{2} V_{carmU} [\alpha - m \sin(\omega t + \delta)] \approx V_{carmU} m_U$$

(1)

$$V_{armL} \approx \frac{1}{2} V_{carmL} [\alpha + m \sin(\omega t + \delta)] \approx V_{carmL} m_L$$

(2)

where $V_{carmU}$ and $V_{carmL}$ are the sums of the upper and lower arm capacitor voltages, which must be regulated such that $V_{carmU} = V_{carmL} = V_{carm}^* \geq V_{dc}$ (where $V_{carm}^*$ is the rated arm capacitor voltage). The DC modulation index is defined as $\alpha = V_{dc}/V_{carm}^*$, and $m_U$ and $m_L$ are the upper and lower arm modulation functions respectively.

For HB-MMC the DC modulation index ‘$\alpha$’ varies narrowly around 1 because of the nature of unipolar SMs being employed (inability to generate negative voltages at the SM or the arm levels). In contrast, FB MMC permits DC modulation indexes ‘$\alpha$’ to vary widely, in the range of $-1 \leq \alpha \leq 1$.

Controlling the sums of the upper and lower arm capacitor voltages at $V_{carmU} = V_{carmL} = V_{carm}^* \geq V_{dc}$ means the existence of redundant SMs in the MMC arms. Apart from reliability improvement in HB-MMC, these redundant SMs do not offer any added value because of the well-known limitations of the unipolar HB SMs [31, 32]. But in FB and hybrid MMCs, the redundant SMs in their arms can offer additional features such as over-modulation (ability to generate or operate with higher AC side voltage than the HB-MMC). Although hybrid MMC can offer such features during normal operation, sustaining such feature during operation with extremely low DC voltage such as active control during DC short circuit faults requires the number of FB SMs in the arms to be increased, as during such operations, FB SMs alone will be responsible.
for synthesis of the negative arm voltages. Apart from the aspects highlighted above, the fundamental operation and control of the FB and hybrid MMCs remain the same as that of the HB-MMC which has been extensively discussed in report 1 [31]. These differences will be articulated and emphasized throughout this report where appropriate.

2.1.1 Detailed switching model (DSM)

Typical detailed switching models of the FB and hybrid MMCs use in depth representations of the FB and HB SMs (SM capacitors and switching devices), where each power electronics switch mimics the conduction pattern and switching characteristics of its physical equivalent (such as the IGBT and anti-parallel diode). For instance, when the arm current defined in Fig. 3(a) is assumed to be positive, the basic operation of the FB SM could be summarised as follows:

- Switching devices $S_1$ and $S_2$, and $S_3$ and $S_4$ that constitute two independent legs represent two complementary pairs, i.e., turning on switch $S_1$ precludes switch $S_2$ from being on and vice versa. The same logic applies to the complementary pair $S_3$ and $S_4$.

- When $S_1$ is on and $S_3$ is off, the FB SM in Fig. 3(b) generates an output voltage $V_{sm}=V_{CSM}$, where $V_{CSM}$ represents the SM capacitor voltage. In this switching state, a positive arm current ($I_{arm}>0$) charges the SM capacitor, while the negative arm current ($I_{arm}<0$) discharges the SM capacitor. Additionally, each switching device in off-state such as $S_2$ and $S_4$ experiences voltage stress equal to capacitor voltage $V_{CSM}$.

- When $S_1$ is off and $S_3$ is on, the FB SM in Fig. 3(c) generates an output voltage $V_{sm}=-V_{CSM}$. In this switching state, a positive arm current ($I_{arm}>0$) discharges the SM capacitor, and negative arm current ($I_{arm}<0$) charges the SM capacitor. Also, both switching devices in off-state such as $S_1$ and $S_4$ experience voltage stress equal to $V_{CSM}$.

- When both switches $S_1$ and $S_3$ are on (or off), the FB SM in Fig. 3(d) and (e) generates an output voltage $V_{sm}=0$. In this switching state, both positive and negative arm currents do not affect the SM capacitor voltage.

- When all switching devices ($S_1$, $S_2$, $S_3$ and $S_4$) are gated off during blocking state as shown in Fig. 3(f), both positive and negative arm currents shown in red and blue find path through the anti-parallel diodes of the switches $S_1$, $S_2$, $S_3$ and $S_4$ and charge the SM capacitor.

As in HB-MMC case described in report 1 [31], DSM accounts for each IGBT turn-on and turn-off times and its on-state resistance and voltage drop (threshold and current dependent component), and other characteristics that define the conduction of the IGBTs and diodes. Such exhaustive representation necessitates the use of stiff solvers with small time steps leading to very longer simulation times, high computation burden, and large memory requirement.

2.1.2 Switching function model (SFM)

As stated in report 1 [31], the switching function modelling methods represent each IGBT and its anti-parallel diode by an ideal switch that denotes the on and off states by 1 and 0 respectively. Considering Fig. 4(a) as the $i^{th}$ FB SM in the MMC arm, its output voltage ($V_{smi}$) can be expressed in terms of the SM capacitor voltage ($V_{CSMi}$) and switching states of the two upper (or lower) switches $S_1$ and $S_3$ as:
Similarly, the switching SM capacitor current of each SM can be related to MMC arm current by:

\[ i_{csmi}(t) = (S_{i1} - S_{i3}) I_{armi}(t) \]  

\[ i_{csmi}(t) = (S_{i1} - S_{i3}) I_{armi}(t) \]  

And the SM capacitor voltage can be calculated at each time step as

\[ V_{CSMi}(t) = \frac{1}{C_{SM}} \int_{0}^{t} i_{csmi}(t) dt \]  

\[ V_{CSMi}(t) = \frac{1}{C_{SM}} \int_{0}^{t} i_{csmi}(t) dt \]  

Equation (3) is transformed into discrete form using Tustin (trapezoidal integration method) as:

\[ V_{CSMi}(t) = V_{CSMi}(t - \Delta t) + \frac{\Delta t}{2} \frac{\Delta t}{C_{SM}} \left[ I_{csmi}(t) + I_{csmi}(t - \Delta t) \right] \]  

\[ V_{CSMi}(t) = V_{CSMi}(t - \Delta t) + \frac{\Delta t}{2} \frac{\Delta t}{C_{SM}} \left[ I_{csmi}(t) + I_{csmi}(t - \Delta t) \right] \]  

The total generic arm voltage is obtained by summing individual SM output voltage as:

\[ V_{arm} = \sum_{i=1}^{N} v_{smi}(t) \]  

\[ V_{arm} = \sum_{i=1}^{N} v_{smi}(t) \]  

Equations (1)-(5) are used to construct the FB-MMC switching function model shown in Fig. 4 (b) and (c). Because switching function modelling method overlooks physical characteristics of semiconductor switching devices (conduction pattern and switching behaviours), realization of blocking state in FB-MMC model in Fig. 4 (c) is achieved by gating off all the IGBTs \( S_1, S_2, S_3 \) and \( S_4 \), and setting the upper and lower
arm modulation functions \( m_U = m_L = 1 \). In contrast, during operation state, the upper and lower arm voltages are realized as:

\[
\begin{align*}
V_{\text{arm}U} &\approx V_{\text{arm}L} \cdot |m_U| \\
V_{\text{arm}L} &\approx V_{\text{arm}U} \cdot |m_L|
\end{align*}
\]

(6)

(7)

In addition, when \( \text{sign}(m_U) \geq 0 \) the switches \( S_1 \) and \( S_4 \) are turned on and \( S_2 \) and \( S_3 \) are turned off, and the opposite is true for \( \text{sign}(m_U) < 0 \). The former scenario arises when FB-MMC arm synthesizes positive voltages, and the latter scenario occurs when the FB-MMC arm synthesizes negative voltages.

Since each arm of the hybrid MMC consists of FB and HB stacks (chain-links), its switching function model is obtained simply by combining the HB-MMC and FB-MMC SFM into one which is shown in Fig. 5. Blocking and de-blocking states of the HB stacks can be realized as described in report 1 [31], and that of the FB stacks can be realized as described above.

Fig. 4: (a) FB SM, (b) SFM of FB SM, and (c) Graphical depiction of SFM of FB-MMC
where $S_{1U}$ and $S_{3U}$ are column vectors of the upper arm switch states for the HB stack; and $I_{csmU}$ and $V_{CSMU}$ are vectors of upper arm capacitor currents and voltages.

$S_{1L}$ and $S_{3L}$ are column vectors of the lower arm switch states; and $I_{csmL}$ and $V_{CSML}$ are vectors of lower arm capacitor currents and voltages.

$S_{xU}$ is the column vector of the upper arm switch states for the HB stack; and $I_{csmU HB}$ and $V_{CSMU HB}$ are vectors of upper arm capacitor currents and voltages of the HB stack.

$S_{xL}$ is the column vector of the lower arm switch states for the HB stack; and $I_{csmL HB}$ and $V_{CSML HB}$ are vectors of lower arm capacitor currents and voltages of the HB stack.

Fig. 5: Graphical depiction of SFM of the hybrid MMC

2.1.3 Thevenin Equivalent model (TEM)

As a follow up to report 1 [31], this section presents Thevenin equivalent models for FB and hybrid MMCs, where the switching devices of the SMs are treated as two-state switched resistances, with on-state and off-state resistances $R_{ON}$ and $R_{OFF}$ respectively, and each SM capacitance is replaced by its electromagnetic transient equivalent circuit.

For a generic SM shown in Fig. 6 (a), the SM capacitor dynamic can be expressed as:
After solving (8) using trapezoidal integration method, the following equations are obtained:

\[
\frac{dV_{CSM}(t)}{dt} = \frac{I_{csm}(t)}{C_{SM}}
\]  

(8)

\[
V_{CSM}(t) = V_{CSM}(t - \Delta t) + \frac{1}{2} \frac{\Delta t}{C_{SM}} \left[ I_{csm}(t) + I_{csm}(t - \Delta t) \right]
\]  

(9)

\[
V_{CSM}(t) = V_{CSM}(t - \Delta t) + R_{csm} I_{csm}(t - \Delta t) + R_{csm} I_{csm}(t) = V_h + R_{csm} I_{csm}(t)
\]  

(10)

where \( \Delta t \) is the simulation time step. The term that represents the calculations in the previous time step is referred to as history term \( V_h = V_{CSM}(t - \Delta t) + R_{csm} I_{csm}(t - \Delta t) \), and \( R_{csm} = \Delta t / 2C_{SM} \) represents the electromagnetic equivalent resistance of the SM capacitor.

Fig. 6 (b) shows the equivalent circuit of the FB SM when Backward Euler and Trapezoidal integration methods are employed. This equivalent circuit can be further simplified using Thevenin theory, where the Thevenin voltage and resistance per SM are:

\[
V_{th}(t) = \frac{R_2 R_3 - R_1 R_4}{R_c (R_1 + R_2 + R_3 + R_4) + (R_1 + R_2)(R_3 + R_4)} \times V_h
\]  

(11)

\[
R_{th} = \frac{(R_1 + R_{tx})(R_2 + R_{tx})}{(R_1 + R_{tx} + R_2 + R_{tx})} + R_y
\]  

(12)

where \( R_{tx} = \frac{R_3 R_{csm}}{R_3 + R_4 + R_{csm}} \), \( R_y = \frac{R_4 R_{csm}}{R_3 + R_4 + R_{csm}} \) and \( R_c = \frac{R_4 R_{csm}}{R_3 + R_4 + R_{csm}} \).

The switched voltage to be developed across each arm can be calculated by:

\[
V_{arm} = \sum_{i=1}^{N} V_{sni}
\]  

(13)

Fig. 6 (c) summarises per phase implementation of the Thevenin equivalent model of FB-MMC, where the SM capacitor dynamics and full converter behaviours during blocking and de-blocking are fully accounted for. Handling of blocking state during DC fault in the Thevenin equivalent FB-MMC model is similar to that of the SFM described earlier.

The Thevenin Equivalent model of the hybrid MMC shown in Fig. 7 is obtained by combining the HB and FB MMC Thevenin equivalent models.

2.1.4 Averaged Model (AM)

The developments of the average models are motivated by the need to have computationally efficient models suitable for wide range of power system studies. Since fundamentally, HB, FB and hybrid MMCS are adhered to practical the same operating principle during normal operation, the same assumptions made in the development of the HB-MMC averaged model apply to the FB and hybrid MMCS. In other words, the systematic derivations of the averaged models of the FB and hybrid MMCS from the first principles are identical to that of the HB-MMC. The added features of the FB and hybrid MMCS are realizable by incorporating additional power electronics switches to mimic their physical behaviours during converter blocking and when their arms require to generate negative voltages. On these grounds and for the avoidance
of duplications, the averaged models of the FB and Hybrid MMCs will be presented in this section without detailed derivations.

Fig. 6: Thevenin equivalent model of the FB-MMC
Fig. 7: Thevenin Equivalent model of hybrid MMC

Fig. 8 (a) and (b) depict per arm averaged models of the HB and FB MMCS [10, 13, 15, 19], where the upper and lower arm voltages $V_{\text{varm}U}$ and $V_{\text{varm}L}$ and equivalent upper and lower arm capacitor currents $i_{\text{cap}U}$ and $i_{\text{cap}L}$ are approximated by:

$$V_{\text{varm}U} \approx \frac{1}{2} V_{\text{carm}U} [\alpha - m \sin(\alpha + \delta)] \approx V_{\text{carm}U} m_U$$

$$V_{\text{varm}L} \approx \frac{1}{2} V_{\text{carm}L} [\alpha + m \sin(\alpha + \delta)] \approx V_{\text{carm}L} m_L$$

$$i_{\text{cap}U} \approx \frac{1}{2} i_{\text{varm}U} [\alpha - m \sin(\alpha + \delta)] \approx i_{\text{varm}U} m_U$$

$$i_{\text{cap}L} \approx \frac{1}{2} i_{\text{varm}L} [\alpha + m \sin(\alpha + \delta)] \approx i_{\text{varm}L} m_L$$

Recall that the realization of the blocking state in a HB-MMC model in Fig. 8 (a) is achieved by adding the auxiliary devices $S_x$ and $D_m$ [19]. In FB-MMC model in Fig. 8 (c), blocking state is realized by gating off all IGBTs $S_1$, $S_2$, $S_3$ and $S_4$, and setting the upper and lower arm modulation functions $m_U = m_L = 1$ (the
same as in FB-MMC SFM and Thevenin equivalent model). The upper and lower arm voltages during de-block state are realized as:

\[ V_{\text{armU}} \approx V_{\text{carmU}} |m_U| \]  
\[ V_{\text{armL}} \approx V_{\text{carmL}} |m_L| \]  

In conjunction with (18) and (19), the auxiliary switches S₁ through S₄ are operated as follows:

a) When \( \text{sign}(m_U) \geq 0 \), the switches S₁ and S₄ must be turned on and S₂ and S₃ must be turned off.

b) When \( \text{sign}(m_U) < 0 \), the switches S₁ and S₄ must be turned off and S₂ and S₃ must be turned on.

The scenario in (a) arises when the FB-MMC arm synthesizes positive voltages during normal operation with rated DC voltage, while a scenario in (b) occurs when the FB-MMC arm synthesizes negative voltages as required during operation with extremely low DC voltage and operation with negative DC voltage.

It is worth to recall that the hybrid MMC facilitates normal and reduced DC link voltage operation and active control of DC fault current during pole-to-pole DC fault (zero DC voltage) by inserting the same number of SM capacitors with positive and negative polarities as that of the FB-MMC. Also, with the assumption that the HB and FB SMs of the hybrid MMC have same capacitances, insertion of the FB SM capacitors with positive polarities will exhibit the same behaviours at SM and arm levels as that of the HB SMs. This fact justifies the use of per arm averaged model depicted in Fig. 8(b) to represent the hybrid MMC (or mixed-SM MMC), provided that the DC modulation control range is restricted as described above \((-\frac{1}{2} \leq \alpha \leq 1\) ), and upper and lower arm modulation functions \(m_U\) and \(m_L\) are set to 0.5 during converter blocking.

![Diagram](image)

Fig. 8: (a) Enhanced per arm averaged model of the HB-MMC, (b) Enhanced per arm averaged model of the FB and hybrid MMCs.

2.2 Control

In broader terms, the FB and hybrid MMCs discussed in this report employ the control systems of the HB-MMC described in report 1 [31] with modifications to cater for the operation during reduced DC voltage. Fig. 9 summarises the overall systems employed in this report to control both FB and hybrid MMCs. Details of the control functions of each loop as follows:

1) The outer controller on d-axis regulates active power or DC voltage and sets positive sequence d-axis current order. Likewise, the outer controller on q-axis regulates reactive power or AC voltage and sets positive sequence q-axis current order.
2) The negative sequence current orders on d- and q-axes are set to zeros (to ensure that a balanced three-phase output currents are drawn or injected into the AC grid during normal conditions and asymmetric AC faults).

3) The inner current controllers on both d- and q-axes regulate positive and negative sequence currents and limit current contribution from the converter to AC fault by regulating the AC components of the modulation functions.

4) Circulating current suppression controller is implemented on per phase basis to suppress the 2nd order harmonic currents in each arm of the FB and hybrid MMC in an effort to reduce semiconductor power losses and SM capacitor voltage ripples.

5) Horizontal and vertical SM capacitor voltage controllers are implemented to ensure equal SM voltage distribution across the three phase legs of the FB and hybrid MMCs, and across the upper and lower arms of each phase leg.

6) The most inner layer is the non-distributed SM capacitor voltage balancing and modulator (not applicable for average models) that ensure the total voltage imposed across each FB or hybrid MMC arm is equally shared between the SM capacitors of the arm and generates the desired arm and output voltages by selecting correct number of SM capacitors to be inserted into power path and bypassed in each instant.
7) An averaged capacitor voltage controller is also implemented to strictly control the sum of the capacitor voltages of the 6 arms at a specific level. In addition, this controller enables the SM capacitors to maintain their voltages around the rated voltage during operation under extremely low DC voltages by drawing small active power from the AC grid to feed system losses.

8) Active DC fault controller is implemented as a standby which can be activated during DC short circuit fault to enable precise control of DC fault current at zero or any desired values (e.g. for fast extinguishing arc).

9) To enable DC voltage control over a wide range, i.e. from rated positive value to zero for hybrid MMC, and from rated positive to rated negative values for FB-MMC, the DC modulation index is designed to be varied with the reference DC link voltage.

3 Real-time Simulation Models

Fig. 10 shows a generic layout of the real-time models of the FB and hybrid MMC models implemented in RSCAD using dual time steps (multi-rate). Parts of the FB and hybrid MMC models that operate at high switching frequency are built in small time-step (i.e. 1.4-2.5µs), whilst the AC grid source is modelled in a larger time step (i.e. 50 µs).

![Real-time Simulation Models Diagram](image)

Fig. 10: A single terminal MMC system modelling method in RTDS

3.1 Power Circuit and Control System Modelling

On the basis of detailed discussions of the FB and hybrid MMCs modelling presented in section 2, real-time user-defined 20-SM FB-MMC SFM and FB-MMC AM, and hybrid MMC AM are built in RSCAD-RTDS simulation platform. The developed models in this report are validated against a number of offline models developed in PSCAD-EMTDC:

- FB-MMC: 20-SM SFM, Thevenin equivalent, and AM.
- Hybrid MMC: AM.

The number of SMs in the developed RSCAD-RTDS model can be easily scaled and modified if more details are required and sufficient RTDS modelling hardware capability are available.

In RTDS platform, the power circuit part of the FB and hybrid MMC models (SFM and AM) and their associated components such as the DC side circuit and interfacing transformer are modelled in the small time step of 2.5µs. While the parts that calculate the SM capacitor dynamics and control systems are placed in a large time-step of 50µs. The user-defined components that implement calculations of SM capacitor
dynamics and voltage balancing are realised in MATLAB-SIMULINK and then converted to RSCAD using code generation with the help of the real-time embedded coder that can optimise the generated codes for a number of objectives such as code efficiency, RAM usage, traceability, etc. The whole real-time simulation model of the test system is implemented on one RTDS rack, with a two-processor PB5 card and three GPC cards (two processors each). One processor on the PB5 card is assigned for total network solution, whilst the other is assigned for the control system. Each converter requires one GPC processor to solve the power circuit that operates at the small time-step. Since this report aims to validate the MMC behaviours under a number of operating conditions, the DC side of the half-bridge MMC is modelled by a stiff DC voltage source connected to two 50km short DC cables each modelled by one pi-section. The AC side is placed at large time-step of 50μs, and the connection between the AC system at large time-step and the MMC power circuit and its DC side components at small time-step is realised through the VSC interface transformer.

3.2 Modelling Challenges

Generally, the two platforms (PSCAD-EMTDC and RTDS-RSCAD) use slightly different approaches in the modelling of some electrical components. For example, switching devices are modelled in different ways and the primary and the secondary winding configurations of the interface transformer in RTDS are different compared to the transformer model in PSCAD. Many of the RTDS models have been tuned empirically in attempt to achieve a better compromise between accuracies, numerical stability, adherence to the fundamentals of discrete simulations, and to minimize the unintended consequences of the introduced delays for facilitating data exchange between different processors and components that operate at different speeds. The accumulated influences of these modelling differences between the offline and real-time simulation platforms may lead to small mismatches in the simulation results of the two platforms.

Table 1 Test system parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MMC rated apparent power (Sn)</td>
<td>1265MVA</td>
</tr>
<tr>
<td>MMC rated active power (P)</td>
<td>±1200MW</td>
</tr>
<tr>
<td>MMC rated reactive power(Q)</td>
<td>±400MVAr</td>
</tr>
<tr>
<td>MMC nominal DC Voltage (Vdc)</td>
<td>640kV(±320kV)</td>
</tr>
<tr>
<td>MMC rated AC output voltage (L-L)</td>
<td>360kV</td>
</tr>
<tr>
<td>Arm inductance (Laarm)</td>
<td>0.13pu</td>
</tr>
<tr>
<td>SM capacitance (Csm) [20-SM MMC]</td>
<td>628µF</td>
</tr>
<tr>
<td></td>
<td>Averaged model 31.4µF</td>
</tr>
<tr>
<td>Nominal Frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>Transformer rated apparent power</td>
<td>1265MVA</td>
</tr>
<tr>
<td>Interfacing transformer voltage ratio</td>
<td>400/360kV</td>
</tr>
<tr>
<td>Transformer leakage reactance</td>
<td>0.18pu</td>
</tr>
<tr>
<td>Transformer resistance</td>
<td>0.004452pu</td>
</tr>
</tbody>
</table>
4 Test system

This section uses one MMC converter terminal to validate the real-time and offline FB and hybrid MMC models. The different models are:

- **FB-MMC**
  - Offline: Switch function model (SFM), averaged model (AM), and Thevenin equivalent model (TEM) provided by PSCAD.
  - Real-time: SFM and AM

- **Hybrid MMC**
  - Offline: AM
  - Real-time: AM

The system in Fig. 11 is modelled in PSCAD and RTDS, with full sets of controllers described above, and detailed system parameters listed in Table 1. The SM capacitances of the FB and hybrid MMC models are calculated based on the same minimum inertia constant of 30ms (or 30kJ/MVA). High impedance AC side grounding is adopted which defines the insulation level of the DC side in practical systems.

![Figure 11: Illustrative test system (power, current and voltage polarities marked in this figure are assumed to be positive)](image-url)
5 Validation of Real-Time Simulation Models against Off-Line Equivalent

It is worth recapturing that the previous reports [31, 32] have shown that the numbers of SMs in the MMC arms have negligible impacts on MMC dynamic behaviours. Therefore, this report presents the detailed validation of the real-time FB-MMC models (20-SM SFM and AM) and AM of hybrid against offline FB-MMC models (20-SM SFM, TEM and AM) and AM of the hybrid MMC respectively. As demonstrated in report 1 [31] that neither the operating conditions, e.g. active/reactive power, system strength, nor MMC operating mode, e.g. power control, AC voltage control, influence the results of validation or leads to divergence of the models. Therefore, most of the validation studies presented in this report will consider the scenario of strong AC grid (SCR=10) and a small number of operating conditions and control modes when the MMCs operate at rated active powers of 1200 MW. The validation scenarios are listed below:

1) Full-bridge MMC validations
   - Normal operation
   - Three-phase symmetrical AC fault
   - Pole-to-pole DC short circuit fault with converter blocking
   - Pole-to-pole DC short circuit fault with active control of fault current is activated.
   - Pole-to-ground DC fault
   - DC voltage reversal
2) Hybrid MMC validations
   - Pole-to-pole DC short circuit fault with converter blocking
   - Pole-to-pole DC short circuit fault with active control of fault current is activated.
   - Pole-to-ground DC fault

5.1 Simulation Scenarios of FB-MMC

5.1.1 Normal Operation

Fig. 12 summarises simulation waveforms of the offline and real-time user-defined FB-MMC when it operates as a power controlling converter using the control systems depicted in Fig. 9. The acronyms PA, PS and PP, and RS and RA displayed in the legends attached to simulation waveforms stand for offline PSCAD AM, SFM and TEM, and real-time SFM and AM respectively. During 0 to 1s, the FB-MMC maintains both its active and reactive power at zeros. At \( t=1\)s, active power is ramped from 0 to 1200MW at a rate of 2400MW/s, while reactive power is maintained at zero.

Fig. 12(a)-(f) show the full-scale and zoomed offline and real-time simulation waveforms of the three-phase currents at the grid (PCC1) and converter side of the interfacing transformer, and MMC upper and lower arm currents. These waveforms show the AC side waveforms obtained from the offline and real-time simulation models are identical, while arm currents exhibit very small and diminishing differences during power ramps, with all arm current waveforms become identical as system settles. The plots for the sums of the capacitor voltages displayed in Fig. 12(g) and (h) show similar behaviour observed in the arm currents, i.e., very small differences in the sums of the capacitor voltages during power ramps but convergence to
identical settling points as the system approaches steady-state. The traces of the active powers, and DC link voltages and currents displayed in Fig. 12(i), (j) and (k) are almost identical, including during transition between two operating points.

In summary, Fig. 12 shows all the offline and real-time simulation models being compared are capable of reproducing the dynamics of the FB-MMC as it varies its power set-points, with negligible errors. Thus, the developed user-defined offline and real-time FB-MMC models (SFM, TEM and AM) are well suitable for studying different dynamics that may arise during normal operation of FB-MMC.
5.1.2 Three-Phase-to-Ground AC Fault

Fig. 13 displays simulation waveforms during a three-phase-to-ground AC fault, with results of the real-time simulations (20-SM SFM and AM) superimposed on that of the PSCAD offline simulations (20-SM SFM, TEM and AM). In the pre-fault, during fault and post-fault conditions, active and reactive powers set-points are maintained at 1200 MW and 0 MVAr respectively. At $t=4s$, a temporary solid symmetrical three-phase-to-ground AC fault is applied at PCC1, with 300ms fault duration.

Fig. 13 (a) and (b), (c) and (d), and (e) and (f) show a full-scale and zoomed simulation waveforms for the three-phase AC voltages at PCC1, three-phase AC currents at the PCC1, converter side of the interfacing transformer. All zoomed waveforms are captured around the instant of fault inception. These waveforms show that the real-time and offline models of the 20-SM SFM, AM and TEM exhibit the same behaviours in terms of trend and magnitude during steady-state and transient conditions.

Likewise, the plots for the upper and lower arm currents displayed in Fig. 13(g) and (h) are almost identical with negligible errors appear briefly in the first few peaks of the arm current following the occurrence of the AC fault, but quickly disappeared. The plots for the sums of the upper and lower capacitor voltages in Fig. 13(g) and (h) indicate that the different models exhibit similar behaviours during steady-state and transients, with extremely small errors appearing at the instances of fault inception and clearance. Fig. 13 (k), (l) and (m) show that the real-time and offline simulation waveforms for the active power, and DC link voltage and current during the three-phase-to-ground AC fault are similar with marginally differences appear briefly around the instants of fault inception and clearance.
A detailed comparison of the real-time and offline simulation results shown in Fig. 13 confirm the accuracies of the developed offline and real-time used defined FB-MMC models (SFM and AM) and their suitability for studying three-phase-to-ground AC faults.
Fig. 13: Simulation waveforms with different FB-MMC models during a three-phase-to-ground AC fault

5.1.3 Pole-to-Pole DC Short Circuit Fault with Converter Blocking

Fig. 14 presents simulation waveforms when a solid pole-to-pole DC short circuit fault is applied at FB-MMC DC terminals at \( t=5 \) s, as shown in Fig. 11, and the converter is blocked 50\( \mu \)s after fault inception (real-time waveforms obtained from 20-SM SFM and AM are superimposed on the offline waveforms obtained from PSCAD 20-SM SFM, TEM and AM). In pre-fault condition, the FB-MMC was operating with a rated active power of 1200MW and zero reactive power.

Fig. 14 (a), (b) and (c) show simulation waveforms for the three-phase AC voltages at PCC1, and three-phase AC currents the MMC injects into PCC1 and converter side of the interfacing transformer respectively, all expanded snapshots around the instant of fault inception. These traces show that all the AC side waveforms (currents and voltages) of the real-time and offline simulations are identical. Similarly, the real-time and offline upper and lower arm current waveforms displayed in Fig. 14 (d) do not exhibit any visible errors in steady state and during the DC fault. The real-time and offline simulation plots for the sums
of the upper and lower arm SM capacitor voltages compared in Fig. 14 (e) also exhibit identical behaviours during steady state and fault periods, and the same can be observed for the active powers, and DC link currents and voltages as shown in Fig. 14 (f), (g) and (h). The results displayed in Fig. 14 confirm the appropriateness of the presented offline and real-time user-defined FB-MMC models for studying pole-to-pole DC short circuit faults when converter blocking is activated.

Fig. 14: Simulation waveforms with different offline and real-time FB-MMC models (SFM, TEM and AM) during DC short circuit fault when converter blocking is activated after 50µs from fault inception
5.1.4 Pole-to-Pole DC Short Circuit Fault with Active Control of DC Fault Current

Fig. 15 presents simulation waveforms when a solid pole-to-pole DC short circuit fault is applied at FB-MMC DC terminals at \( t=3 \) s, and fault control is enabled after 50\( \mu \)s from fault inception. In pre-fault condition, the FB-MMC was operating with a rated active power of 1200MW and zero reactive power.

Fig. 15(a) and (b) display simulation waveforms for the pole-to-pole DC voltage and DC current. The plots displayed in Fig. 15 (a) and (b) show that the FB-MMC manages to quickly control DC fault current to zero, with all models exhibit similar behaviours during steady-state and DC fault, including during the transition between the two states. The plots for the arm currents and sums of the SM capacitor voltages shown in Fig. 15 (c), (d), (e), and (f) show full agreements between the models being compared. These simulation waveforms show that the arm currents and SM capacitor voltages of the FB-MMC are well-controlled during pole-to-pole DC short-circuit fault.

Fig. 15 (g) - (k) show the three-phase AC currents the MMC injects at PCC1 and converter side of the interfacing transformer, and the three-phase voltages at PCC1. These traces show that all the AC side waveforms (currents and voltages) of the real-time and offline simulations match well. The arm, converter and grid currents become practical zero during DC short circuit fault when the MMC fault control is enabled to regulate the DC current to zero with zero active power as shown in Fig. 15 (l). In the simulation, reactive power during the DC fault is also maintained at zero but can be controlled at different values if required.

In summary, the results of detailed validation displayed in Fig. 15 confirm the appropriateness of the presented offline and real-time user-defined FB-MMC models (SFM, TEM and AM) for the study of pole-to-pole DC short circuit faults when fault current control is enabled.
Fig. 15: Simulation waveforms for different offline and real-time FB-MMC models (SFM, TEM and AM) during DC short circuit fault when fault controlled is enabled after 50µs from fault inception

5.1.5 Pole-to-ground DC Fault

Fig. 16 shows simulation waveforms when a pole-to-ground DC fault occurs at t=2s, and the DC voltage is controlled to be half of the rated value 0.6s after the fault inception in order to reduce the DC voltage stress on the healthy pole.
Fig. 16 (a), (b), (c) and (d) show offline and real-time simulation waveforms for the pole-to-pole and pole-to-ground DC voltages and DC link currents. The plots for DC voltages and current exhibit brief disturbances which are associated with the discharge of the faulted pole and charging of the healthy pole, and with both simulation platforms and different models show almost identical behaviours. Observed that halving of the pole-to-pole DC link voltage 0.6s from fault inception reduces the voltage stress on the healthy pole to the rated design value of 320kV. The post-fault DC current remains the same as the pre-fault value and system now transmits half of the rated power.

The plots for the three-phase currents and voltages measured at grid and converter side displayed in Fig. 16 (e), (f), (g), (h), (i), (j), (k) and (l) indicate that the pole shift during pole-to-ground DC fault only affects the converter side voltage, and has no impact on the converter and grid side AC currents and grid voltages. See that the reduction of the DC link voltage helps to reduce the DC voltage stress being exposed to insulations of the low-voltage windings of the transformer compared to equivalent HB-MMC described in report 1 and 2 [31, 32]. All the behaviours described above are reproduced accurately in the results of the offline and real-time simulations shown in Fig. 16 (e) through (l).

Fig. 16 (m), (n) and (o) shows samples of upper and lower arm voltages $v_{armUA}$ and $v_{armLA}$, when the MMC operated with rated and half DC voltage. Observe that the arm voltages ($v_{armUA}$ and $v_{armLA}$) vary between 0 and $V_{dc}$ as DC modulation index varies narrowly around 1 during operated with rated DC voltage, and portions of the arm voltages ($v_{armUA}$ and $v_{armLA}$) cross to negative during operation with half DC voltage as DC modulation index varies around $-\frac{1}{2}$. These behaviours are in line with the control system and modulation of the FB-MMC designed and described in Section 2. Fig. 16 (p) and (q) show that the arm currents of the FB-MMC remain well-controlled during pole-to-ground DC fault when pole restraining (halving of the DC voltage) is enabled, with all offline and real-time use defined models being compared are able to reproduce different dynamics of the arms as expected. Fig. 16(r) presents the active power of the FB-MMC exchange with the AC grid at PCC1 during normal operation and pole-to-ground DC fault, and observe that all the models being compared reproduce identical results.

Additional simulation case that demonstrates fast execution of pole-restraining during pole-to-ground DC fault has been shown in Fig. 21 in appendix.
5.1.6 DC Voltage Reversal

Fig. 17 presents offline and real-time simulation waveforms when the FB-MMC initiates its DC voltage reversal at $t=2.6s$, from 640kV to -640kV, within 0.4s. Prior to the DC voltage reversal, at $t=2.15s$, the FB-MMC reduces its active power exchange with the AC grid from 1200MW to 0 within 0.25s and held it at 0. At $t=3s$, the FB-MMC starts the restoration of its active power exchange with the AC grid from 0 to 1200MW within 0.5s (during this period the FB-MMC operates with rated DC voltage of -640kV). During the entire operating period, the FB-MMC maintains its reactive power exchange with the AC grid constant at 300MVar.

Fig. 17 (a) and (b), (c) and (d) show the simulation waveforms for the positive and negative pole DC voltages, DC current, and active and reactive powers the FB-MMC injects into PCC1. These waveforms show that different offline and real-time models of the FB-MMC produce practically the same results. The results confirm the ability of these models to reproduce the bipolar operation of FB-MMC and
uninterruptable STATCOM functionality, independent of the DC link voltage. Similarly, the plots for the upper and lower arm voltages shown in Fig. 17 (e) and their zoomed version when the FB-MMC operates with -640kV displayed in Fig. 17 (f) show identical results, with the DC modulation index $\alpha = -1$ (equivalent to $-\frac{1}{2}V_{dc}$) as anticipated. Same can also be observed for the currents the FB-MMC injects into AC grid at PCC1 and the upper and lower arm currents displayed in Fig. 17 (g) and (h), and (i) and (j). The plots for the sums of the upper and lower SM capacitors of different offline and real-time models of the FB-MMC being compared in Fig. 17 (k) and (m) also indicate a good match for the results produced by the models during steady-state and transients.
Fig. 17: Simulation waveforms that compare the transient behaviours of the user-defined offline and real-time FB-MMC models (SFM, TEM and AM) during DC voltage reversal

5.2 Simulation Scenarios of the Hybrid MMC

5.2.1 Pole-to-Pole DC Short Circuit Fault with Converter blocking

Fig. 18 presents simulation waveforms when a permanent solid pole-to-pole DC short circuit fault is applied at DC terminals of the hybrid MMC at \( t=5 \) s, and converter blocking is activated 50\( \mu \)s after the fault inception. In this validation, real-time waveforms of the AM are superimposed on that of the offline PSCAD AM. In pre-fault condition, the hybrid MMC was operating with a rated active power of 1200MW and -200MVAr.

Fig. 18(a) and (b) show that both offline and real-time AMs of the hybrid MMCs produce identical pole-to-pole DC voltage and DC link currents, with the drop of the DC link current slightly slower than that of the FB-MMC presented and discussed in Section 5.1.3, due to the lower counter voltages the hybrid MMC SM capacitors present to oppose or suppress the arm and output phase to currents to zeros, see Fig. 18(c) and (g). Fig. 18(d) shows that in the process of suppressing the arm and output currents to zeros, the sums of the SM capacitor voltages of the hybrid MMC exhibit substantial over-charging compared to that of the FB-MMC presented in Section 5.1.3, for the same pre-fault conditions and the instant of fault inception. Fig. 18 (e) and (f) show active and reactive powers the hybrid MMC exchanging with the AC grid, and it can be seen that both active and reactive powers drop to zero quickly after activation of converter blocking.

Simulation waveforms displayed in Fig. 18(a) to (g) show that the developed offline and real-time user-defined AMs of the hybrid MMC produce the expected behaviours with sufficient accuracies, and therefore,
the models are suitable for detailed DC short circuit fault studies, particularly, when DC fault reverse blocking capability to be activated.

Fig. 18: Simulation waveforms with offline and real-time hybrid MMC AM models during DC short circuit fault when converter blocking is activated.
5.2.2 Pole-to-Pole DC Short Circuit Fault when Fault Control is Enabled

Fig. 19 presents simulation waveforms when a solid pole-to-pole DC short circuit fault is applied at the DC terminals of the hybrid MMC at \( t=3 \) s, and fault control is enabled 50\( \mu \)s after fault inception. Fig. 19 (a) and (b) show pole-to-pole DC link voltage and DC current in the positive pole. These waveforms show the offline and real-time simulation models produce identical results during the DC short circuit fault, with the hybrid MMC is able to control the DC fault at zero in a similar way as that previously demonstrated with the FB-MMC in Section 5.1.4. Fig. 19 (c) and (d) and (h) and (i) show the upper and lower arm currents, and three-phase currents the hybrid MMC injects into PCC1 at grid side. These waveforms show while the hybrid MMC controls DC fault current at zero during the DC short circuit fault, it retains full control over the reactive exchange with the AC grid, see Fig. 19 (k). The AC currents observed in the arms and output circuits of the hybrid MMC are associated with the reactive power being exchanged with the AC grid. The symmetry of the arm currents is an evidence of the STATCOM operation of the hybrid MMC during DC short circuit fault. Fig. 19 (f) and (g) display the sums of the SM capacitor voltages of the hybrid MMC, and these plots indicate that the hybrid MMC retains full control over its SM capacitors. Fig. 19(j) shows the active power that the hybrid MMC exchanges with the AC grid, and it drops to zero during DC fault as expected. The results shown in Fig. 19 confirm that the hybrid MMC is able to control fault current during pole-to-pole DC short circuit fault as the FB-MMC, but this is achieved in hybrid MMC at significantly lower semiconductor losses compared to the FB-MMC.

In summary, simulation waveforms presented in Fig. 19 confirm the validity of both offline and real-time user-defined AMs of the hybrid MMC to perform detailed studies of DC short circuit fault when fault current control is enabled.
5.2.3 Pole-to-Ground DC Fault

Fig. 20 shows simulation waveforms when a pole-to-ground DC fault occurs at t=2s, and the DC voltage is halved 0.6s after the fault inception in order to reduce the DC voltage stress on the healthy pole.

Fig. 20 (a), (b) and (c) show the offline and real-time simulation waveforms for the pole-to-ground and pole-to-pole DC voltages and DC link currents. The plots for the DC voltages and current show brief disturbances due to discharging and charging of the capacitors of the faulted and healthy poles. Both models display almost identical behaviours during the pole-to-ground DC fault. Similar to the previous study with FB-MMC, halving of the pole-to-pole DC link voltage reduced the voltage stress on the healthy DC cable to its pre-fault value of 320kV and allowed the post-fault DC link current to remain the same as in the pre-fault condition at rated. Again, active and reactive power traces in Fig. 20 (d) and (e) show that the hybrid manages to ride-to-through a pole-to-ground DC fault in the same manner as FB-MMC with 50% active.
power transfer at rated DC current, while its reactive power exchange with the AC grid remains unaffected. The plots for the upper and lower arm currents, three-phase currents measured at grid side, and sums of the SM capacitor voltages displayed in Fig. 20 (f) and (g), (h) and (i), and (j) and (k) also confirm the validity of the two developed models.

Additional simulation case that demonstrates faster execution of pole-restraining during pole-to-ground DC fault has been shown in Fig. 22 in appendix.
6 High-level Comparison between HB-MMC, FB-MMC and Hybrid MMC

Error! Reference source not found. presents a global comparison of the key features and shortcomings between the HB, FB and hybrid MMCs, with special attention paid to aspects that may affect system performance. Although FB-MMC is known for its high semiconductor losses, this comparison and detailed quantitative studies presented above show that it offers the most features and largest control range. However, in the context of the present trend of voltage source converter based multi-terminal HVDC links, hybrid MMC offers the best overall trade-offs between efficiency and performance; especially, as it offers all FB-MMC features except DC voltage reversal. Error! Reference source not found. lists selected waveforms to further highlight the differences between the converters being compared.
Table 2: High-level comparison between HB-MMC, FB-MMC and hybrid MMC assuming all converter topologies have the same DC link voltage, use the same IGBTs [31, 33-38]

<table>
<thead>
<tr>
<th>Features</th>
<th>HB-MMC</th>
<th>FB-MMC</th>
<th>Hybrid MMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor losses</td>
<td>Low (0.5-0.7)%</td>
<td>High (1.19-1.2)</td>
<td>Medium (0.82-1.1)</td>
</tr>
<tr>
<td>Maximum inductive reactive power capability</td>
<td>Limited by device current rating</td>
<td>Limited by device current rating</td>
<td>Limited by device current rating</td>
</tr>
<tr>
<td>Maximum capacitive reactive power capability</td>
<td>Limited by DC voltage and device current rating</td>
<td>Limited by DC voltage and device current rating</td>
<td>Limited by DC voltage and device current rating</td>
</tr>
<tr>
<td>AC fault ride-through capability</td>
<td>Yes, including symmetrical and asymmetrical AC faults</td>
<td>Yes, including symmetrical and asymmetrical AC faults</td>
<td>Yes, including symmetrical and asymmetrical AC faults</td>
</tr>
<tr>
<td>Continued operation during pole-to-ground DC fault</td>
<td>No, as healthy pole will be exposed to excessive voltage stress</td>
<td>Yes, as it offers pole restraining capability that keeps the voltage stress on the healthy DC cable at rated</td>
<td>Yes, as it offers pole restraining capability that keeps the voltage stress on the healthy DC cable at rated</td>
</tr>
<tr>
<td>Continued operation during pole-to-pole DC short circuit fault</td>
<td>No</td>
<td>Yes, with full control over DC fault current and AC side currents (reactive power), but with zero DC or active power transfer</td>
<td>Yes, with full control over DC fault current and AC side currents (reactive power), but with zero DC or active power transfer</td>
</tr>
<tr>
<td>Fault blocking capability</td>
<td>No</td>
<td>Yes, but in weak AC grid this may cause voltage stability issues due to a sudden loss of reactive power support from the converter</td>
<td>Yes, but in weak AC grid this may cause voltage stability issues due to a sudden loss of reactive power support from the converter</td>
</tr>
<tr>
<td>DC Voltage reversal</td>
<td>No</td>
<td>Yes, this feature is well suited for operation in DC grids that contain LCC converters.</td>
<td>No</td>
</tr>
</tbody>
</table>
Table 3: Selected waveforms to highlight the differences between HB-MMC, FB-MMC and hybrid MMC

<table>
<thead>
<tr>
<th></th>
<th>AC faults</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HB-MMC</strong></td>
<td><img src="image1.png" alt="Waveform" /></td>
<td>AC current can be controlled</td>
</tr>
<tr>
<td><strong>FB-MMC</strong></td>
<td><img src="image2.png" alt="Waveform" /></td>
<td>Converter blocking</td>
</tr>
<tr>
<td><strong>Hybrid MMC</strong></td>
<td><img src="image3.png" alt="Waveform" /></td>
<td>Fault control is enabled, and reactive power is controlled at zero.</td>
</tr>
</tbody>
</table>
Fault control is enabled, and reactive power is controlled at \(-200\text{MVAr}\). 

<table>
<thead>
<tr>
<th>Pole-to-Ground DC fault</th>
<th>HB-MMC</th>
<th>Healthy pole experiencing DC over-voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FB-MMC</td>
<td>Pole-to-pole DC voltage is reduced to 50%</td>
</tr>
<tr>
<td></td>
<td>Hybrid MMC</td>
<td>Pole-to-pole DC voltage is reduced to 50%</td>
</tr>
</tbody>
</table>

7 Conclusions
This report has validated a number of real-time user-defined models of the FB and hybrid MMCs, particularly, the SFM and AM against several offline PSCAD user-defined models of FB and hybrid MMCs, namely, the SFM, AM and TEM. Results of comprehensive comparisons of the simulation waveforms (offline overlaid on the real-time) show that the offline and real-time simulation waveforms are in full agreement during normal operation and various AC and DC faults conditions. It has shown that the FB and hybrid MMCs can provide full control of DC and AC current during DC faults conditions. The
developed models can be used for a variety of system studies with high computational efficiency and accuracy examining the enhanced control and operation provided by FB and hybrid MMCs.

8 Appendix

Besides models’ validations, detailed illustrative simulation waveforms presented in subsections 5.1.5 and 5.2.3 have demonstrated the capacity of FB and hybrid MMC to initiate a pole-restraining function during a pole-to-ground DC fault to reduce the voltage stress on the healthy pole and facilitate continued operation with 50% of the DC voltage and 50% of the rated power.

Therefore, this appendix presents two additional simulation cases when a faster execution of pole restraining during pole-to-ground DC faults are adopted, considering the FB and hybrid MMCs.

The simulation time-scales have been used in these illustrations are:

- In pre-fault, both FB and hybrid MMCs operate with 1200MW and -200MVAr.
- The negative DC cable is subjected to a permanent pole-to-ground at t=2s.
- After 1ms from fault inception (t=2.001s), both FB and hybrid MMCs initiate a pole restraining process first by quick reduction of active power order from 1200MW to 600MW, while reactive power order remains unchanged at -200MVAr.
- At 7ms from fault inception (t=2.007s), both FB and hybrid MMCs initiate a rapid reduction of DC voltage from 640 kV to 320 kV, within 10ms.
Fig. 21: FB-MMC simulation waveforms demonstrating a quick execution of a pole restraining during pole-to-ground DC fault

Fig. 21 and Fig. 22 display real-time RTDS simulation waveforms obtained from the user defined AMs of the FB and hybrid MMCs. The traces for active and reactive powers, positive and negative DC voltages, DC current, and AC currents in the grid side and shown in Fig. 21(a) through (f) and Fig. 22 (a) through (f) show that both the FB and hybrid MMCs offer pole restraining function that can be initiated within a short time from the occurrence of a pole-to-ground DC fault in order to curb the voltage stress on the insulation of the healthy DC cable, and ensure compatibility with the safe clamping times of commercial surge arresters.
Fig. 22: Hybrid MMC simulation waveforms demonstrating a rapid execution of a pole restraining during pole-to-ground DC fault.
References


