The National HVDC Centre Scottish & Southern Electricity Networks	***Project*: High power DC/DC converter and DC hub design based on Modular Multilevel topology**

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Title :	Design of high power MMC bridge operating at medium frequency		

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Acronyms

UoA	University of Aberdeen
SSE	Scottish and Southern Energy
MMC	Modular Multilevel Converter
SM	submodule
HBSM	Half Bridge SM
FBSM	Full Bridge SM
HVDC	High voltage direct current
EP	Energy to power ratio
CCSC	Circulating current suppression controller
PWM	Pulse with modulation
NLM	Nearest level modulation
SHE	Selective harmonic elimination
THD	Total harmonic distortion
ADC	Analog to digital converter

Abstract

This report presents the results of first task of the project "**High power DC/DC converter and DC hub design based on Modular Multilevel topology**". The main objective of this task is designing of a high power MMC bridge working at medium frequency (0.2-1kHz) and verifying the design results using an appropriate MMC bridge model in PSCAD.

This MMC bridge will then be used in DC/DC converter and DC hub. Therefore this design document provides guidelines to determine the main parameters of a MMC bridge for DC/DC converter and DC hub applications. These parameters are:

- Number of Phases
- Number of levels
- Operating frequency
- Submodule topology (Half-bridge or Full-bridge)
- Arm inductance and capacitance
- IGBT switches
- Modulation and Voltage balancing algorithms
- Processing resources

This report has been configured in 4 main chapters. Chapter 2 discusses the selection of above parameters except number of levels and operating frequency. In this chapter, the number of phases, the submodule type and the modulation technique are fixed and lower limits for the SM capacitance and arm inductance are given. A short discussion on IGBT switch and processing resource is also included. A significant part of this chapter is dedicated to developing suitable module voltage balancing algorithm where two algorithms are selected and compared on detailed PSCAD model.

Chapter 3 presents a harmonic analysis for LCL DC-DC converter. Based on the results of this analytical study, a lower limit on the number of SMs will be selected. As AC voltage quality is not major concern in DC/DC and DC hub design, the minimum possible number of levels is preferred to enable converter design at higher operating frequencies.

Chapter 4 is focused on final design and simulation verification. In this chapter, the design parameters are fixed based on the power losses, SMs voltage capacitors ripple and also the ripple on DC voltage and current. A detailed PSCAD model is developed and converter operation is confirmed for typical operating conditions.

It is concluded that the 1000MVA, ±320kV MMC should have 20 cells in each arm, and the recommended operating frequency is 300Hz. The MMC converter is expected to have around 0.7% losses, and the total DC/DC converter losses are estimated to be around 1.5%.

1. Introduction

1.1 Background

The VSC HVDC has been in operation in around 15 projects worldwide since 1998 [1],[2]. It has also been employed for interconnecting 400MW BorWin offshore wind farm (2009) and two further similar projects, 800MW DolWin 1 and 2 (in 2013) are in construction. So far, VSC HVDC has been exclusively employed as 2-terminal system with underground cables. The advantages and operating principles of VSC HVDC are becoming well known and accepted.

Over the years, the limitations of HVDC technology have been emerged. In particular, the questions have been raised of optimal topologies when multiple HVDC lines are located in a small geographical area. Such scenario occurs as an example with multiple wind farms in an offshore area. Because of limitations on DC cable size and maximum single-injection point there is further opportunity for interconnecting offshore DC lines to increase operating flexibility and system security. In order to avoid transferring from one DC system to another through an AC system there would be benefit in connecting directly one DC line to another and to build a DC grid.

The existing state of HVDC technology does not facilitate development of meshed DC grids. Modern DC transmission grids will be built using 2 or multilevel VSC AC/DC converters which are vulnerable to DC faults. DC fault currents can reach very high magnitudes in very short time. Some equipment manufacturers have made good progress on developing fast DC circuit breakers based on power electronics, yet these are not commercially available. However there are open challenges related to fault current magnitude, discriminative fault detection on long DC lines, overall coordination of DC grid protection and component costs.

In recent years, a parallel research has been progressing on fault tolerant high-power DC/DC converters [3],[4]. Most DC/DC converters can limit the DC fault current and isolate the fault using only local measurements (no need for grid wise coordination). Also, they provide DC voltage stepping and power flow control and therefore they can become essential component in building DC grids.

The DC/DC concept based on non-isolated inner passive circuits has shown encouraging performance and the concept has been proven on a small prototype [3]. However the non-isolated DC/DC may require new approach in overall DC grid protection and earthing. The isolated DC/DC converters provide more flexibility and they are better suited for direct connection with the existing monopolar or bipolar HVDC systems.

The DC/DC converters have not been implemented at high power and they require much further design/development research and hardware demonstration.

1.2 DC/DC topologies and motivation for study

The LCL DC/DC converter has demonstrated promising performance with low losses and weight in initial studies [3],[4]. This topology adjusts DC voltage symmetrically around central point and therefore it is suitable for symmetrical monopole or bipolar HVDC, but it is not suitable for monopolar systems. A very important positive property is the inherent current regulation in case of DC faults. Another important advantage is the capability to operate at high frequencies (since air core inductors are used) and therefore size will be reduced. The lack of galvanic isolation limits the application of this topology.

A similar topology is dual active bridge DC/DC converter with internal AC transformer. In this topology an internal AC transformer is used which provides galvanic isolation. Grounding on one DC side is independent of grounding on the other DC side. The response to DC faults on either side is generally good since in any case one bridge sees a fault on AC side and can avoid fault penetration to the healthy DC side by the action of control system or tripping IGBTs. However the internal AC transformer always takes fault currents and therefore high inductances are required. Also the fault response relies on the fast control and protection of the two bridges. This topology has limited capability to adjust DC voltage (it has essentially fixed stepping ratio) but this property is not normally required with transmission applications.

In either of the above DC/DC topologies the reference studies have been focused on 2-level VSC for the internal AC/DC bridges. The recent HVDC technology advances have demonstrated benefits of MMC topologies and they are becoming exclusive topology for 50/60Hz VSC terminals [5]-[8].

This project will explore the DC/DC converter design using MMC technology. The main challenge is linked with the higher frequency operation since DC/DC internal circuit is expected to operate in mid frequency range 100-1000Hz. The DC/DC converter design will involve complex optimization of MMC bridges and the internal passive circuit (LCL or transformer) by observing the crucial performance indicators like steady-state and transient responses, and DC faults while minimizing weight and losses. It is estimated that a high power DC/DC converter will become commercially attractive if the total losses are below 2.5%, and if the weight is comparable with 50/60Hz AC/DC converter connected to an isolation transformer.

1.3 Medium frequency MMC AC/DC bridge design

The first task of this project aims developing suitable medium frequency AC/DC MMC converter. This converter will be the basic building block for MMC based DC/DC converters and for multiport DC hubs.

A high power MMC has only been designed and studied for 50/60Hz applications. The challenges of developing MMC for medium frequency operation include:

- Selecting optimal operating frequency to minimize losses and footprint,
- Selecting appropriate number of cells,
- Passive component design (submodule capacitance and arm inductance),
- Control processing resource demand and limitations,
- Sub module voltage balancing algorithm selection,
- Minimization of harmonics, on both AC and DC side

This study will address the above challenges using analytical approaches in the first stage. Analytical conclusions give general recommendations and formulae which will enable future designs in similar applications. The analytical results will provide a range of design parameters in order to reduce scope of trial and error on detailed simulators.

The MMC converter design will be finalized using detailed modeling on professional simulation platform EMTDC/PSCAD. The aim is to optimize all parameters for a 1000MVA, ±320kV MMC converter and to estimate converter size and losses. The MMC converter operation will be confirmed for steady-state and transient for power reference reversal and DC faults.

2. MMC Design

In this chapter, a high power medium frequency MMC bridge for DC/DC converter and DC hub applications will be designed. The main parameters of MMC are selected based on theoretical guidelines first. The design results will be finalized and verified by detailed simulations obtained from PSCAD model of the converter. Simulation results are employed to optimize the converter design with the main objective of minimum loss and size.

Such MMC will be one port in DC/DC converter or DC hub which will be developed in next reports.

2.1 Design requirements and parameters

The MMC bridge will be designed to be used in DC/DC converter with rated power 1000MVA and DC voltage ±320 KV. The main design parameters that need to be determined are listed below:

- Sub Module type,
- Number of phases,
- Number of levels,
- Operating frequency,
- Arm capacitance,
- Arm inductance,
- IGBT module,
- Modulation technique,
- Voltage balancing algorithm,
- Processing resources,

The above parameters should be determined based on design requirements and objectives which are mainly:

- Minimising power losses,
- Minimising costs,
- Minimising weight,
- Minimising volume,
- Minimising harmonics,

For an MMC, the ripple on the SMs capacitor voltages is expected to be less than 10% []. For a DC-DC converter including two MMCs and one internal LCL circuit (or transformer), the total power losses are expected to be less than 2.5% while the cost, weight and volume should be as minimum as possible. It may not be possible to optimize all the above objectives simultaneously and a tradeoff should be made.

The main sources for power losses are the switching and conduction losses of the MMC SMs, the conduction losses in the arm inductors, and the conduction losses in the internal AC circuit of the DC-DC converter.

Minimizing the cost is an objective that is usually considered in the design process. However, this report will consider only the cost of power losses as well as some of the MMC components that have direct impact on the power losses including SMs capacitors, arm inductors and internal LCL circuit components.

The weight and volume of MMC based DC-DC converters are mainly of interest for offshore applications due to space and weight critical limitations in harsh working environments.

Generally, the MMC and DC-DC converters are part of a DC grid. Therefore, the harmonics should be minimized to: 1) reduce the power losses corresponding to these harmonics and 2) prevent the propagation of these harmonics to other part of the DC grid.

In this chapter and after a brief description of MMC operation, an MMC bridge will be analytically designed considering given requirements and objectives. All the converter design parameters except number of cells and operating frequency will be studied in this chapter.

2.2 MMC Principles of Operation

The schematic of a 3-phase MMC is shown in Figure 2.1. The converter is composed of 3 phases (or legs) where each phase consists of two arms. Each arm is composed of N_{cell} series submodules (SMs) and one arm inductor. The number of AC voltage levels that MMC can generate is equal to $N_{cell}+1$. For example, a 21-level MMC has 20 SMs per arm.

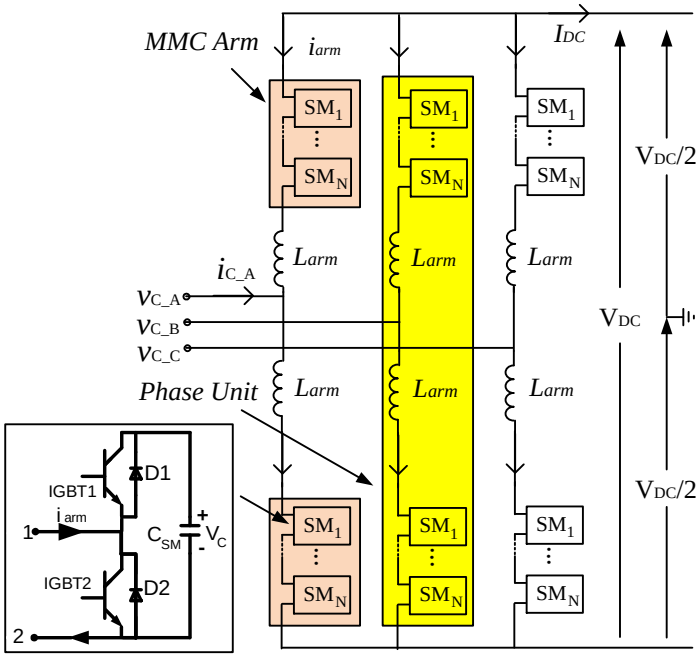

Figure 2.1 Schematic of a 3-phase half bridge MMC

Full bridge and half bridge topologies have been used in SM development. Considering half bridge MMC, each SM involves two HV valves and their anti-parallel diodes and a capacitor C_{SM}. Figure 2.2 shows the four possible operating states of a half bridge SM where each HV valve includes one single IGBT. Figure 2.2 (a and b) shows the states where IGBT1 is ON and IGBT2 is OFF. Figure 2.2 (c and d) shows the states where IGBT1 is OFF and IGBT2 is ON. Table 2.1 summarizes these four cases.

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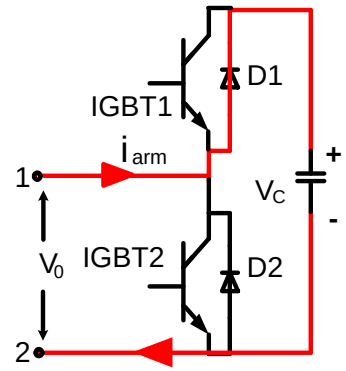
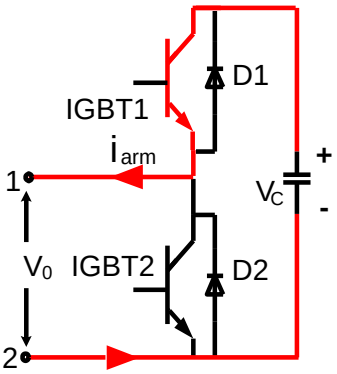
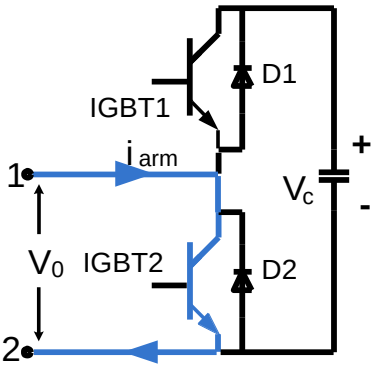


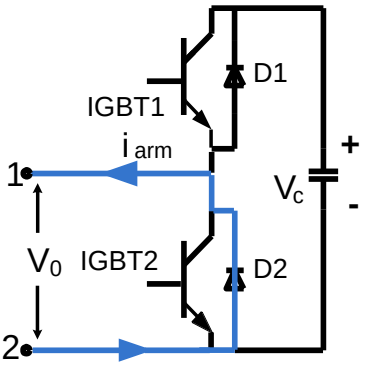
a) IGBT1:ON , IGBT2:OFF (positive current)



b) IGBT1:ON , IGBT2:OFF (negative current)



c) IGBT1:OFF , IGBT2:ON (positive current)



d) IGBT1:OFF , IGBT2:ON (negative current)

Figure 2.2 Four possible operating states of a half bridge SM

Table 2.1 States and current paths of a SM

IGBT1	IGBT2	V_0	Current direction	Current path	Capacitor state
ON	OFF	V_C	$i_a > 0$	D1	charging
ON	OFF	V_C	$i_a < 0$	IGBT1	discharging
OFF	ON	0	$i_a > 0$	IGBT2	unchanged
OFF	ON	0	$i_a < 0$	D2	unchanged

Note that switching both IGBTs will cause SM capacitor short circuit and should be avoided similar to any two level VSC. If both IGBTs in a SM are switched OFF the SM capacitor will be charged. This is useful switching state which can be used at the converter start up or during the DC fault event. This state gives similar circuit of Figure 2.2a or Figure 2.2d depending on the arm current direction. If the arm current is positive, the capacitor will be charged (Figure 2.2a) and if the current is negative, the capacitor voltage remains unchanged (Figure 2.2d).

Figure 2.3 shows the five possible AC voltage levels and corresponding states of the SMs for a 5-level MMC. Figure 2.3a shows the state where all four upper SMs are ON and all four lower SMs are OFF; therefore the upper arm voltage is V_{DC} and the lower arm voltage is zero resulting in the phase

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AC voltage of $-V_{DC}/2$. Figure 2.3b-e show the other AC voltage levels. As is shown in different switching states, N_{cell} SMs in each phase should be triggered at any time.

Note that it is possible to have different combinations of ON and OFF SMs if arm voltage is not equal to V_{DC} or zero (switching states shown in Figure 2.3 b-d). This property is used in SM capacitor voltage balancing which is discussed later.

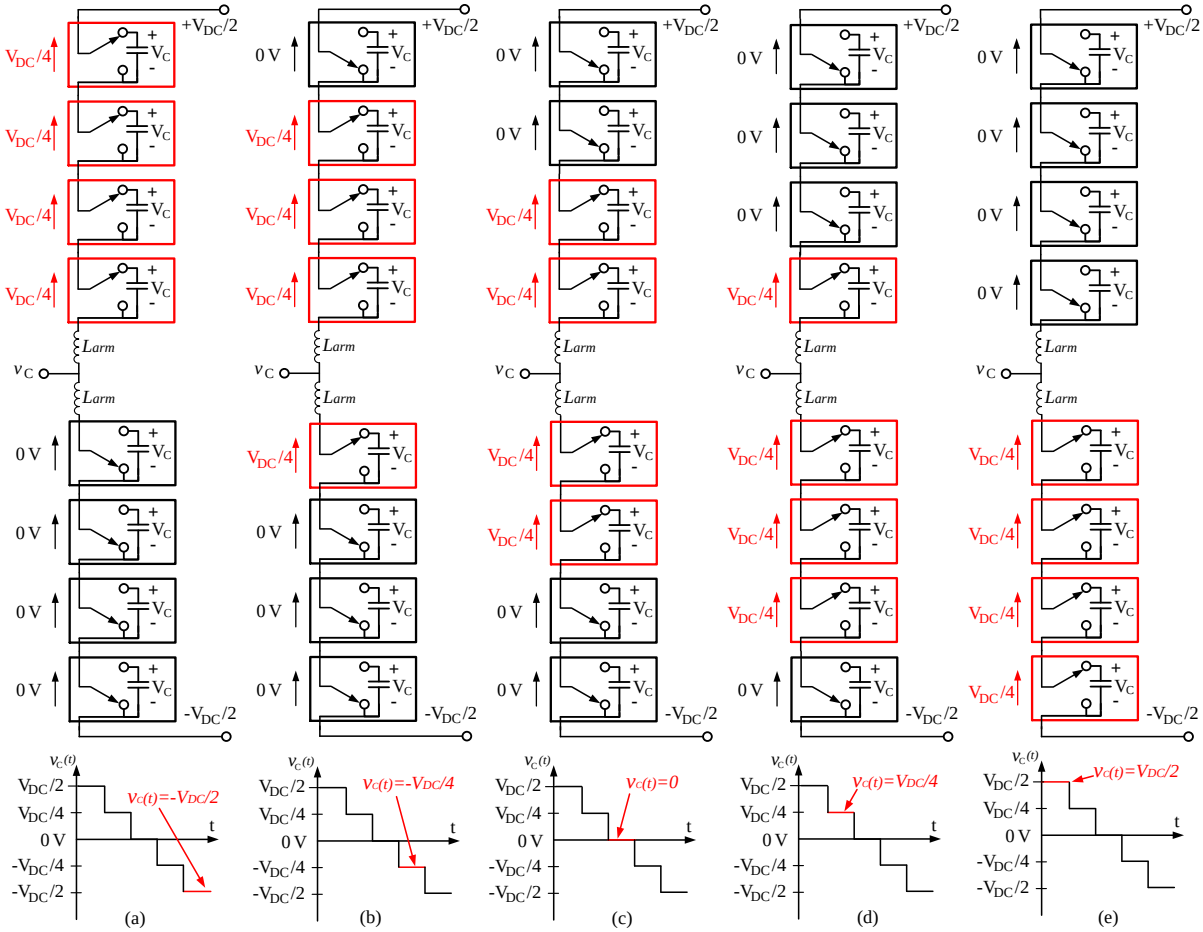

Figure 2.3 AC voltage levels and corresponding SMs states of 5-level MMC

2.3 SM type

Two types of SM can be used in an MMC; 1) Half Bridge SM (HBSM), 2) Full Bridge SM (FBSM). Figure 2.4 shows the schematic of these two SMs. As it is seen, the HBSM uses two IGBT switches (IGBT1 and IGBT2) and their anti-parallel diodes (D1 and D2) while FBSM uses four IGBT switches and their anti-parallel diodes. In practical application, HBSM also includes a thyristor in parallel with diode D2 and a bypass switch.

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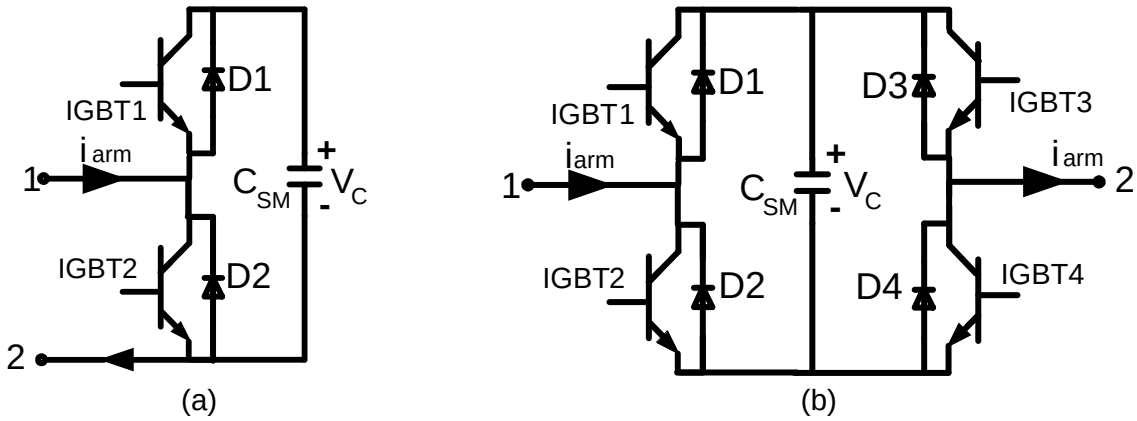

Figure 2.4 HBSM and FBSM

The main advantage of the FBSM is its capability to insert the SM into the circuit with either positive or negative polarity. This gives additional flexibility in controlling the converter and blocking the DC fault current which is a big concern in DC grids. Although this feature is very important in HVDC, it is not crucial for DC-DC converter application. In fact, LCL DC-DC converter has an inherent DC fault blocking and consequently the DC faults cannot propagate from one DC side to the other. This feature will be studied in detail in the next report.

On the down side, the FBSM MMC requires double IGBTs and therefore has cost and power losses almost twice the equivalent HBSM system. This big drawback of FBSM implies that HBSM is selected for DC/DC bridges. From now on and for brevity, every SM means HBSM.

2.4 Number of phases

The number of phases is one of the first items that should be fixed in design process of a converter. The main criteria for selecting number of phases are as follows:

1. Practical power rating per phase

The main criterion for determining the number of phases is the rated power. Practically, the current rating of existing IGBT switches are limited and therefore the transferred power through each phase is 250-350MW which suggests 3 or 4 phases for a 1000MVA MMC converter.

2. Components cost and power losses

Increasing the number of phases implies increasing the number of following components:

- IGBT modules
- Arm inductors
- SM capacitors
- Valve control processing units

Increasing the number of above items has direct impact on the cost of the converter. Although the number of these components will be increased if higher number of phases is selected, the converter cost and power losses may not increase at the same rate for the same power rating. In fact, by increasing the number of phases, the arm current will be decreased. Therefore, lower current rated components can be adopted.

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3. Reliability

Another criterion is the reliability of the system. Having more phases gives a more reliable converter which enables converter to operate even if some of the phases are lost. For example, losing one phase in 4-phase system means operation can continue with ¾ rated power.

4. Common mode voltage

When we are working with 2-level VSC, an even number of phases (for ex. 2, 4, …) is recommended to reject the common mode voltage which increases the cost for higher voltage isolation [1]. For MMC and especially with a reasonable number of SMs (20 and higher), there is no common mode voltage problem and therefore even or odd number of phases can be chosen.

In this phase of the project, we are mostly focusing on the design of a single MMC bridge and therefore we consider a 3-phase MMC which is easier to implement and verify in simulation environment. In fact, we can directly connect the AC side of the MMC to common 3-phase AC grid. In the next phase of this project, we will revise this selection and will consider 4-phase MMC as well and compare the results for 3-phase and 4-phase MMC-based DC-DC converter.

2.5 MMC Main components

In this section, we provide the guidelines for designing the MMC cell capacitance and arm inductance as the main passive components as well as the IGBT modules.

2.5.1 Cell capacitance

The cells' capacitors are the energy storage elements of MMC which are used instead of traditional DC link capacitor in 2-level VSC. For a converter with a given power raring, there is always a trade-off between the capacitor size and the cell voltage ripple; i.e. lower capacitance results in higher cell voltage ripple and vice versa. The cell capacitor is selected to keep the cell voltage ripple within a range of ±10% [5], [2].

In practical converters, the capacitor size is commonly determined using energy to power ratio (EP) which is defined in (2.1). The EP for MMC should be in the range EP=30-40 kJ/MVA. The maximum energy stored in MMC is [6]:

$$EP = \frac{E_{c\max}}{S_n}$$
$$E_{c\max} = 2p * N_{cell} * \left(\frac{1}{2} * C_{SM} * \left(\frac{V_{dc}}{N_{cell}} \right)^2 \right) \quad (1.1)$$

Where, E_{cmax} is the stored energy in the converter, S_n is the nominal power of the converter, N_{cell} is the number of cells per arm, p is number of phases, V_{DC} is the DC link voltage and C_{SM} is the cell capacitor.

Therefore, the cell capacitance can be calculated as:

$$C_{SM} = \frac{EP * S_n}{p * N_{cell} * \left(\frac{V_{dc}}{N_{cell}} \right)^2} = \frac{EP * S_n}{p * N_{cell} * (V_{cell})^2} \quad (1.2)$$

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Where V_{cell} is the cell capacitor average voltage. From (1.2) it can be seen that higher number of cells implies larger SM capacitor.

The problem with the equation (1.2) is that the Impacts of MMV operating frequency and cell capacitor voltage ripple in capacitor design is missing. This is of great importance for this study as the MMC bridge is supposed to be used in DC/DC converter with high operating frequency. In fact both of these two important parameters are hidden in the EP variable shown in (1.1).

Here, we revise the equation (1.2) to include the operating frequency and cell voltage ripple. Consider that the variation of the cell capacitor voltage is in the range of $\pm\Delta V_{cell}$, and therefore the energy variation of one cell is

$$\Delta E_{cell} = \frac{1}{2} C_{SM} \left(\left(V_{cell} + \Delta V_{cell} \right)^2 - \left(V_{cell} - \Delta V_{cell} \right)^2 \right) = 2 C_{SM} * V_{cell} * \Delta V_{cell} \tag{1.3}$$

Considering all cells having similar maximum and minimum voltage variation, the energy variation of an MMC within half a cycle is

$$\Delta E_{MMC} = 2 * p * N_{cell} * \Delta E_{cell} = 4 * p * N_{cell} * C_{SM} * V_{cell} * \Delta V_{cell} \tag{1.4}$$

Therefore, the relation between the energy variation, rated power and operating frequency of an MMC is

$$\frac{\Delta E_{MMC}}{\left(T / 2 \right)} = S_n \Rightarrow S_n = \Delta E_{MMC} * 2 f \tag{1.5}$$

Combining (1.4) and (1.5),

$$C_{SM} = \frac{S_n}{8 p * f * N_{cell} * V_{cell} * \Delta V_{cell}} \tag{1.6}$$

Eq. (1.6) confirms that C_{SM} is inversely proportional to the frequency, cell voltage variation, and number of cells. Comparing (1.6) with (1.2),

$$EP = \frac{1}{8 f \left(\Delta V_{cell} / V_{cell} \right)} \tag{1.7}$$

Note that both sides of the equality (1.7) have the same dimension with the unit of Sec.

It is worthwhile mentioning that the calculated cell capacitance is based on cell capacitors evenly voltage distribution and would be valid if an appropriate voltage balancing algorithm is used. In practical application, running voltage balancing algorithm at high frequency is corresponded with high power losses and is not of interest. Therefore, a larger cell capacitance will typically be selected to reduce the power losses related to the voltage balancing algorithm.

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Example 2.1:

*For a 1000MVA 401-level 3-phase MMC with V_{DC}=640kV, the cell voltage is V_{cell}=640/400=1.6kV. Assuming the cell voltage ripple of ±10%, operating frequency of 50Hz, and number of phases 3, the SM capacitance is obtained C_{SM} =1000/(8*3*50*400*1.6*0.16)≈8.13mF.*

It is clear that if we adopt larger capacitance, the cell voltage ripple will be decreased. For example, C_{SM} =10mF gives the cell voltage ripple around ±7.8%. This cell capacitance can be obtained from eq. (3.2) by assuming EP=30 J/KVA. The equation (1.7) can be also verified by equating f=50Hz and Δ=0.078, which gives the energy power ratio EP=0.032sec=32 J/KVA which is close to the assumed EP (EP=30 J/KVA).

2.5.2 Arm inductance

The arm inductor is designed based on the following criteria:

1) **Limit the circulating current**

This criterion is mainly important if the MMC is not equipped with active circulating current suppression control (CCSC) or the number of SMs is very low. Therefore, for an MMC with active CCSC and high number of SMs, this criterion is not critical.

2) Prevent resonance with the arm capacitance

For a given arm capacitance $C_{arm}=C_{SM}/N_{cell}$, the arm inductance that causes resonance at the frequency ω is given by [6], [7]:

$$L_{arm\_res} = \frac{1}{C_{arm}\omega^2}\frac{2\left(h^2-1\right)+M^2h^2}{8h^2\left(h^2-1\right)} \tag{1.8}$$

Where *h* is the harmonic number and *M* is the modulation index. The arm inductor should be selected larger than L_{arm_res}. The worst case is for h=2 & M=1 where

$$L_{arm\_res} \approx \frac{0.1}{C_{arm}\omega^2} \tag{1.9}$$

3) Limit the DC fault current

In event of DC fault, the arm inductor voltage may rise to V_{dc} suddenly which results in inrush current through the diodes and IGBTs. The arm inductor must be larger than the critical inductance $L_{arm_}$crit to limit the switch and diode current increase rate [2]

$$L_{arm\_cr} = \frac{0.5V_{dc}}{\left(dI_{dc}/dt\right)_{cr}} \tag{1.10}$$

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Where the critical current derivative $\left(dI_{dc}/dt\right)_{cr}$ for diodes and IGBTs is in the range 1-10KA/μs [2].

The condition (1.8) gives much larger L_{arm} than *(1.10)* and therefore the resonance condition (3.8) is commonly considered to determine L_{arm}.

Example 2.2 :

Consider the MMC of example 2.1. For two operating frequencies f=50Hz and f=500Hz, the condition (3.8) gives L_{arm}=40mH and L_{arm}=4mH, respectively (considering C_{arm} is inversely proportional to frequency).

The condition (1.10) with a $\left(dI_{dc}/dt\right)_{cr}$ of 5kA/μs for the above two cases gives L_{arm_cr}=320/5000=62uH. Therefore this condition can be ignored and just condition (1.8)is sufficient for obtaining the minimum arm inductor.

2.5.3 IGBT Module

The IGBT modules are selected based on the converter current and voltage. Generally, a safety factor of **2.0** for voltage and **1.5** for current is applied. This means that in nominal operation, the rated voltage of the IGBT module should be at least **double** the maximum voltage across it and its rated current should be at least **1.5** times larger than the switch rms current. Additionally the peak value of the IGBT should not typically exceed double rated current and this transient high current is typically allowed for 2ms. This criterion usually is checked through the converter modelling in simulation stage.

For MMC of example 2.1, the nominal voltage across each cell is V_{cell}=640/400=1.6kV. Therefore, the rated voltage of selected IGBT module should be larger than 3.2kV.

The arm current has DC component equal to the DC current divided by number of phases (p) and AC component equal to half of phase current. The rms value of the arm current is therefore:

$$I_{arm\_rms} = \sqrt{\left(I_{dc}/p\right)^2 + \left(I_{ac\_rms}/2\right)^2} \qquad (1.11)$$

Where I_{dc} is the MMC DC current, I_{ac_rms} is the rms AC current and p is the number of phases. The DC current is calculated by dividing the rated power S_n=1000MVA with the rated DC voltage V_{DC}=640kV and is obtained equal to 1560A. The rms AC current for full active power and zero reactive power is obtained using the AC power equation $S_n = \sqrt{3}V_{ac}I_{ac}$ and considering line voltage of 380kV gives Iac_rms ≈ 1520 A. As a result, the rms value of the arm current for a 3-phase, 1000MVA, 640kV MMC would be equal to 920A. Therefore, the rated current of the IGBT module should be around 1300A or above.

In summary, we need to select IGBT module with rated voltage and current of 3.2kV and 1.3 kA or higher. It is possible to find single IGBT module with the rated voltage and current for this case with large number of cells, but it would be impossible to find available off the shelf IGBT modules for other applications. For example if the number of cells is decreased to 100 and below, the rated voltage should be larger than 12.8kV which can be only achieved by using a number of series IGBT modules.

Some examples of possible IGBT modules suitable for this study are as below:

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- ABB 5SNA 1300K450300 (4500V & 1300A)
- ABB 5SNA 1500E330300 (3300V & 1500A)
- ABB 5SNA 1200G450300 (4500V & 1200A)

2.6 MMC control

The control of MMC can be divided into two control levels; 1) MMC higher level control, 2) MMC valve (arm) control.

The MMC higher level control is responsible for regulating DC voltage (or active power) and AC voltage (or reactive power). The outputs of MMC higher level control are the MMC arms' reference voltages which are used for valve switching pattern generation. The MMC arm control generates appropriate switching patterns with the objectives of keeping the SMs capacitors voltages within a prescribed range and keeping the total power losses as low as possible.

2.6.1 MMC Higher Level Control

Figure 2.5 shows the block diagram of a typical higher level control for a 3-phase MMC. It involves a master control to achieve control objectives as well as circulating current suppression controller (CCSC) block to mitigate the double frequency current circulation. It measures AC voltages and currents (v_{AC_ABC}, i_{AC_ABC}), DC voltage and current (V_{DC}, I_{DC}), AC active and reactive power (P_{AC}, Q_{AC}), top and bottom arm currents ($I_{arm\_T\_ABC}$, $I_{arm\_B\_ABC}$) and generates the MMC arm reference voltages (V_{ref_TA} - V_{ref_BC}).

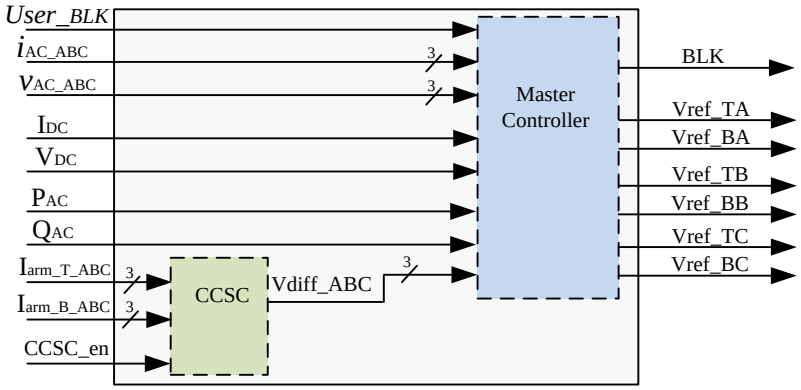

Figure 2.5 Block diagram of MMC higher level control

Figure 2.6 illustrates details of the master control and CCSC. The master control is composed of two cascaded two-level controllers where the inner PI loops control the dq components of AC currents. The outer loops regulate the DC voltage (or active power and partially DC voltage using DC droop control) and the AC voltage (or reactive power and partially AC voltage using AC droop gain). The outputs of these two controllers, M_d and M_q, will be transferred to ABC frame to generate the voltage reference for MMC phases.

All the MMC AC controlled currents are transferred to dq coordinate frame rotating at second harmonic ω as is normal practice for two level VSCs. All the controlled variables (V_{DC}, I_{DC}, V_{AC}, P_{AC}, Q_{AC}, I_{AC_dq}) are filtered before control circuit.

The CCSC block receives the differential currents in d2q2 coordinate frame rotating at second harmonic 2ω, I_{diff_dq2}, and tries to regulate the differential currents to zero using PI controllers. The differential currents I_{diff_dq2}, are obtained by first summing the upper and lower arm currents and then

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transferring the results to d2q2 frame. The outputs of the CCSC in ABC frame will then be added to the output of the master control to generate the final reference voltages.

Note that the structure of the controller shown in Figure 2.6 is usually used for an MMC connected to AC grid. The control structure for a DC-DC converter would be different and will be explained in detail in the next phase of this project.

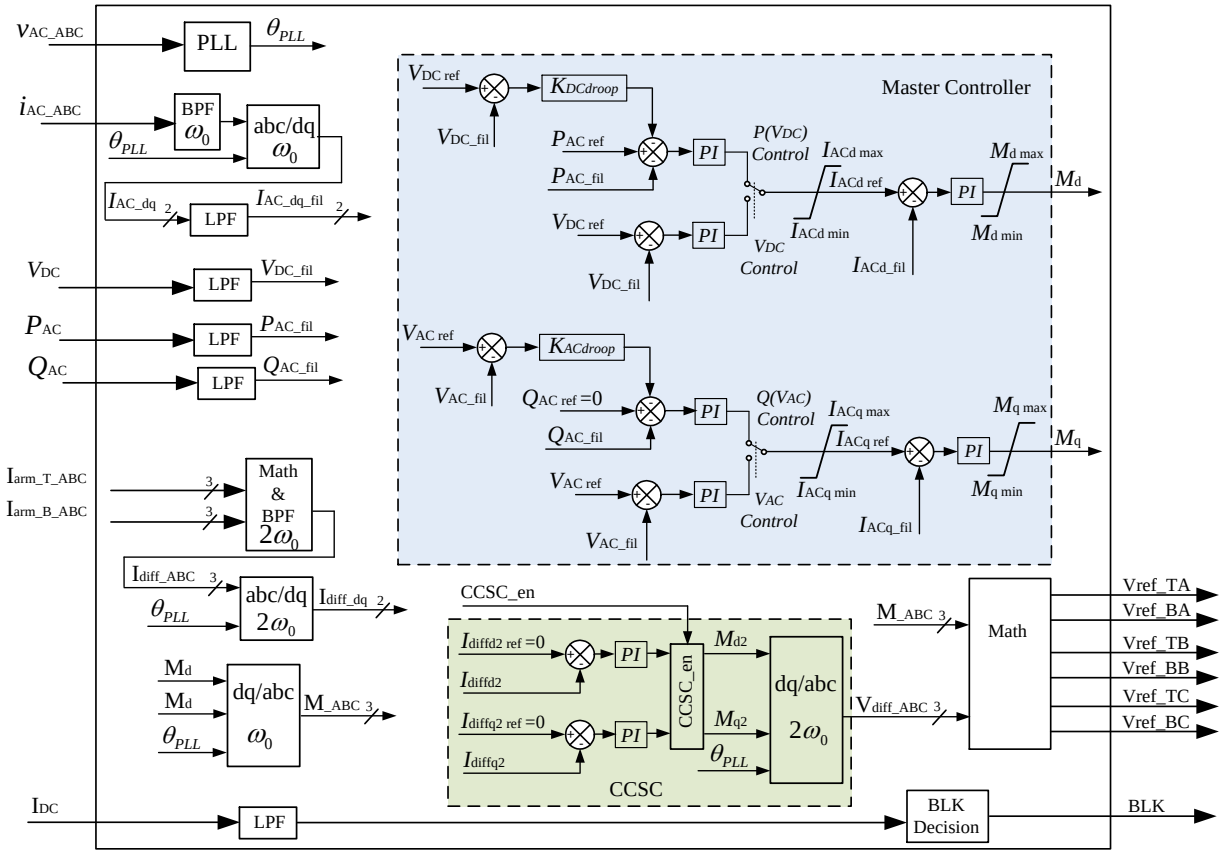

Figure 2.6 Control structure of MMC high level control

2.6.2 MMC arm control

Figure 2.7 shows a schematic of a 3-phase MMC with a dedicated controller for each arm. It is seen that the arm controller receives the arm reference voltage, measures arm currents, and SMs capacitors voltages, and generates the SMs firing pulses. The input BLK is a user control input to block the valve whenever needed (say in the event of fault).

Figure 2.8 shows the block diagram of the MMC SMs switching pattern generation. It comprises of two main blocks; 1) modulation block, 2) voltage balancing block

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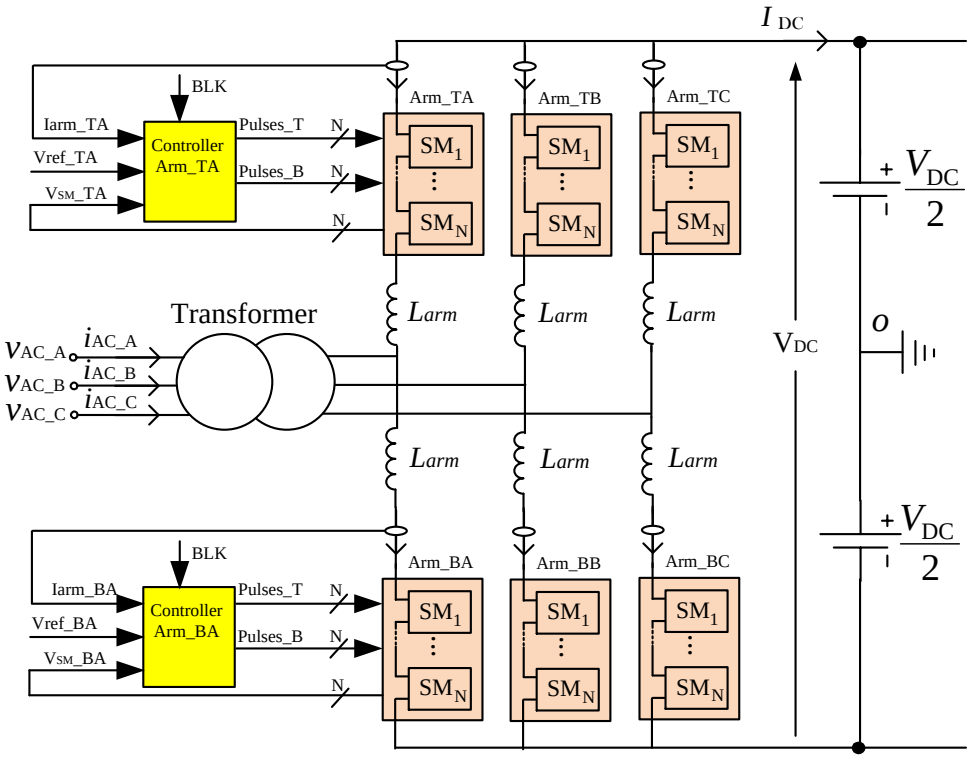

Figure 2.7 Schematic of a 3-phase MMC with arm controllers

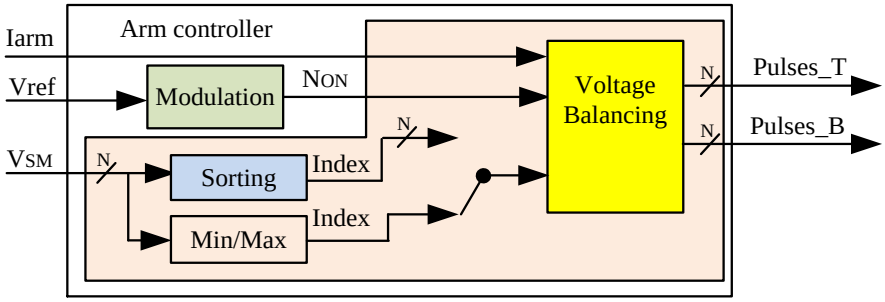

Figure 2.8 Block diagram of MMC arm controller

The input of modulation block is the arm reference voltage and its output is the number of ON SMs, N_{ON}. The voltage balancing block receives N_{ON} and generates the appropriate switching pulses for upper and lower IGBT modules of the SMs within the valve. It receives the measured SMs capacitors voltages, V_{SM} and sorts them in ascending/descending order to find their maximum or minimum. It also uses the measured arm current Iarm as it will be used with the sorted list of cell capacitors to determine which SMs to be inserted. Different methods have bene proposed for MMC cell capacitor sorting which will be shortly discussed later.

2.7 Modulation Techniques

The aim of modulation technique with MMC is to determine the number of ON SMs in each arm for a given reference arm voltage. Figure 2.9 shows common modulation techniques for MMC [2].

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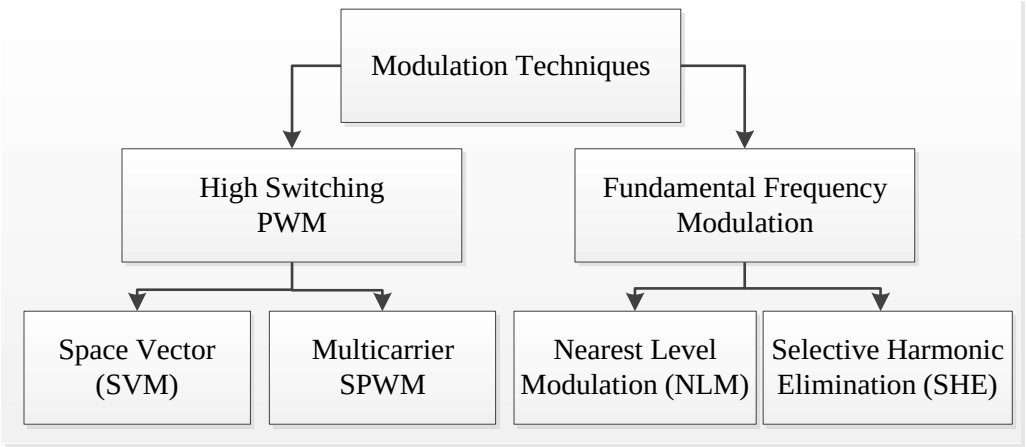

Figure 2.9 MMC modulation techniques

The two common multilevel pulse width modulation (PWM) techniques are space vector and multicarrier based PWM which are extension of conventional two-level PWM strategies [2].

The fundamental frequency modulation techniques are more attractive for high power MMC because of lower switching losses. These staircase multilevel modulation methods can be mainly classified into selective harmonic elimination (SHE) and nearest level modulation (NLM) as shown in Figure 2.9. In SHE method, all switching angles are computed offline, for eliminating harmonics at each value of modulation index and stored in a lookup table, which are then interpolated according to the operating condition. The SHE requires large memory and therefore is not practical if the number of cells is high.

The NLM approximates the desired AC voltage to the closest available voltage level of MMC as illustrated in Figure 2.10. The computation of NLM is simple because it uses just a round function to round up the reference voltage to a nearest available arm voltage level. It is very attractive modulation technique for MMC especially if the number of cells is high.

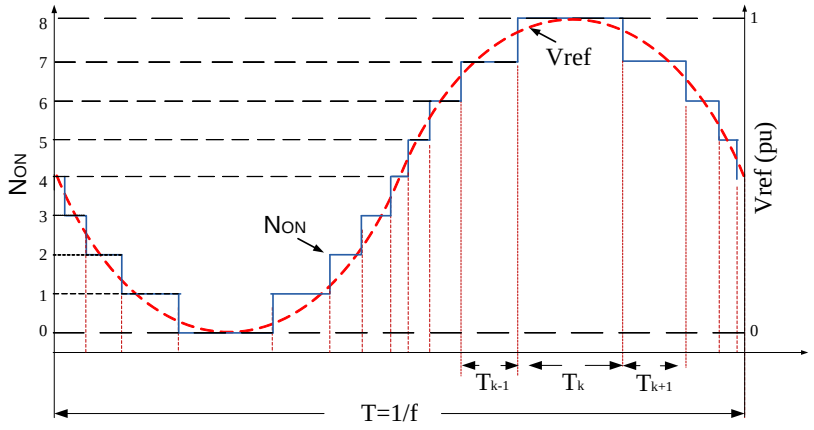

Figure 2.10 Illustration of NLM technique for a 9-level MMC

2.8 Voltage Balancing Algorithms

In order to keep the SMs capacitor voltages close to nominal value (Vdc/Ncell), an appropriate voltage balancing algorithm should be employed. Failure to adequately balance the SMs' voltages not

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only distorts the output voltage but also can result in component damage if individual SMs voltages deviates much above the component rated value.

The capacitor voltage balancing algorithm receives the number of ON SMs (N_{ON}), arm current and SMs capacitor voltages and determines which SMs should be inserted (ON) or bypassed (OFF). Different voltage balancing algorithms have been proposed in the literature [8]-[11]. In this section, the most popular ones will be presented.

2.8.1 Basic Sorting Algorithm

The flowchart of basic voltage balancing algorithm is shown in Figure 2.11. The inputs to the algorithm are the arm current, N_{ON} and the SMs capacitors voltages. It sorts the SMs based on their measured capacitor voltages and determines which SMs should be switched ON considering the arm current direction. If the arm current is positive (based on the direction shown in Figure 2.1), the N_{ON} SMs with the **lowest** voltage levels from the sorted list will be switched ON. This allows the voltage level of these SMs to be increased and results better DC voltage distribution amongst SMs. Alternatively if the arm current is negative, the N_{ON} SMs with the **highest** voltage levels from the sorted list will be switched ON resulting in their voltage levels to be reduced [8].

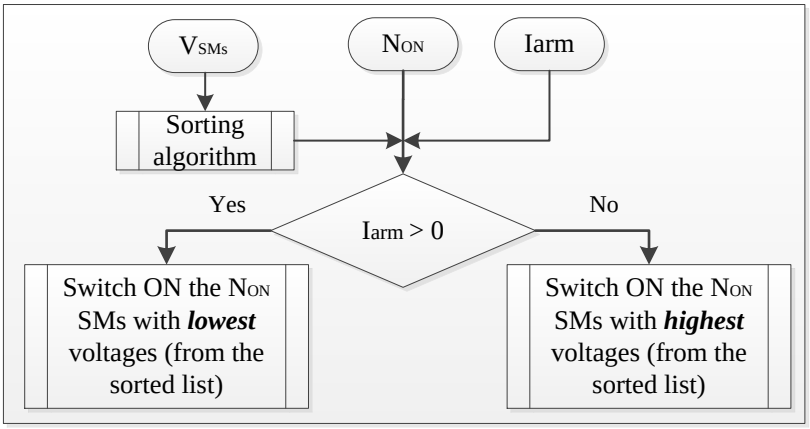

Figure 2.11 Basic voltage balancing algorithm

The basic sorting algorithm gives a low ripple and uniform capacitor voltage distribution for all MMC SMs. However the main problem with this algorithm is the very high switching losses (too many cells are switched at each switching instant) and this is the reason that the basic sorting algorithm is not usually implemented in practical converters.

2.8.2 Sorting Algorithm with changed N_{ON}

Figure 2.12 shows the flowchart of this voltage balancing algorithm [9]. The difference to the previous method is that it applies the voltage balancing of the SMs if and only if the N_{ON} is changed. Therefore, at the first step of the algorithm, it checks if N_{ON} is changed or not. If it is changed, the algorithm finds new N_{ON} SMs that should be switched ON and updates the SMs switching pattern. Otherwise, it keeps the SMs switching patterns unchanged.

It is understood that the switching losses will be extremely decreased compared to the basic sorting algorithm with the cost of higher SM capacitor ripple. However, it will be shown later that the switching losses are still high in particular for high number of cells. In addition, the SMs capacitor

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voltages in this sorting algorithm have higher ripple and are not as uniform as in the previous basic sorting algorithm.

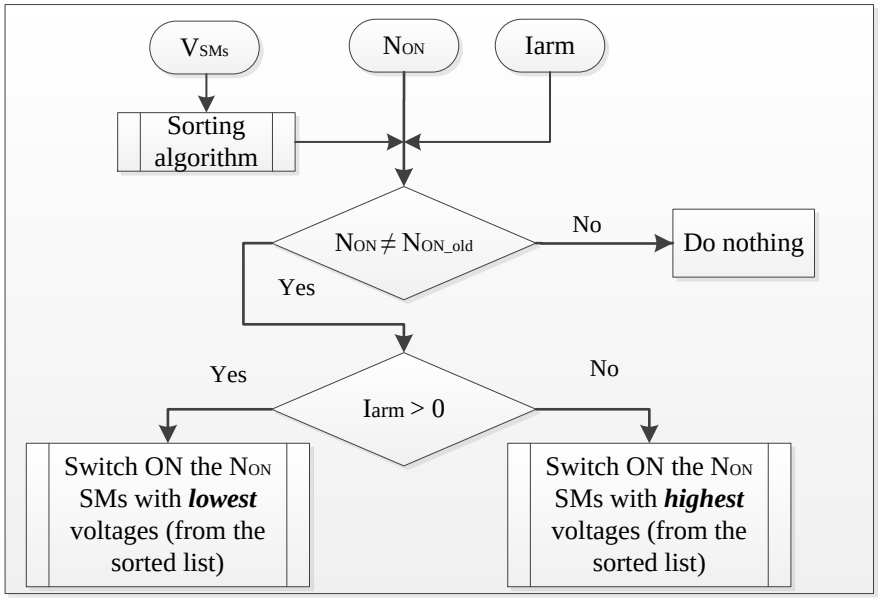

Figure 2.12 Voltage balancing algorithm with changed N_{ON}

Sorting Algorithm with Threshold

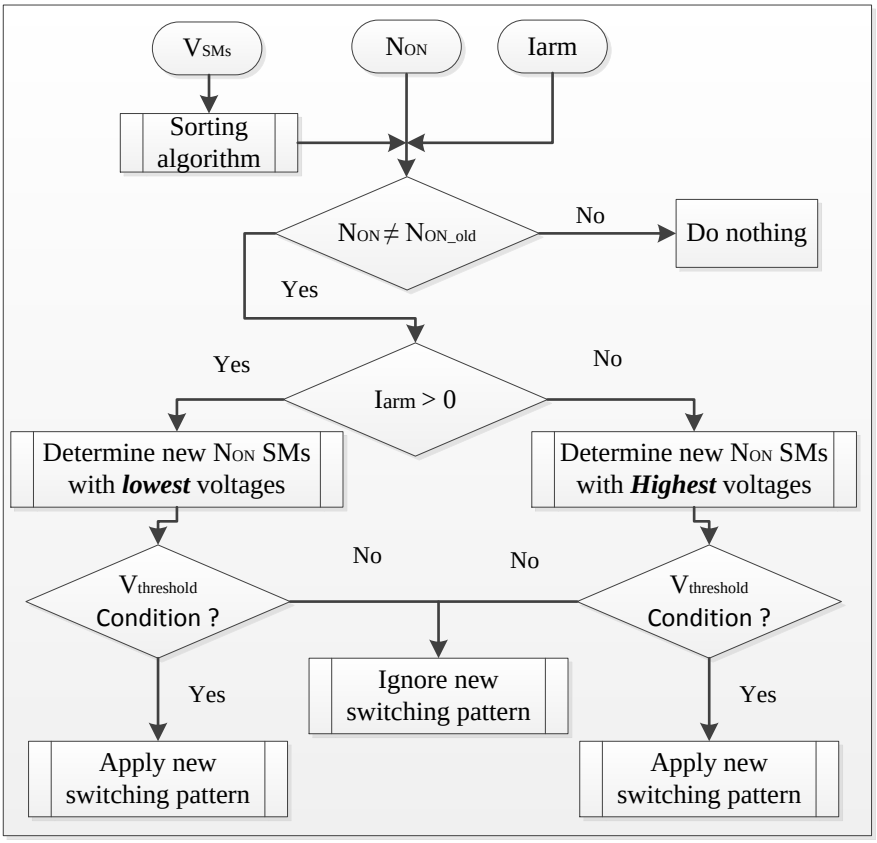

Figure 2.13 shows the flowchart of the sorting algorithm with a voltage threshold. Similar to the sorting algorithm with N_{ON}, this algorithm checks inserted SMs variation (ΔN_{ON}) and keeps the switching pattern unchanged if N_{ON} has not changed.

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The main difference between this algorithm and the sorting algorithm with changed N_{ON} is that it applies an additional condition before changing the SMs switching pattern. After calculation of the new ON and OFF SMs, the algorithm checks the voltage levels of the SMs that are required to change switching state. If the difference between voltage levels of two SMs that are required to toggle switching state (one SM from OFF to ON and the other SM from ON to OFF) are within a prescribed threshold $V_{threshold}$, the new switching pattern will be ignored for these two SMs and their previous switching status will be retained.

Applying the voltage threshold reduces the switching losses at the cost of more deviation in the SMs voltage levels. There is a tradeoff between MMC power losses and SMs capacitors' voltage ripple in threshold selection. The larger voltage threshold results in lower switching losses and larger ripple on SM voltages and vice versa. Therefore, the selection of appropriate voltage threshold depends on the maximum acceptable SM voltage ripple and switching losses. It should be also noted that implementation of voltage threshold condition requires more processing resources which might be a challenging issue.

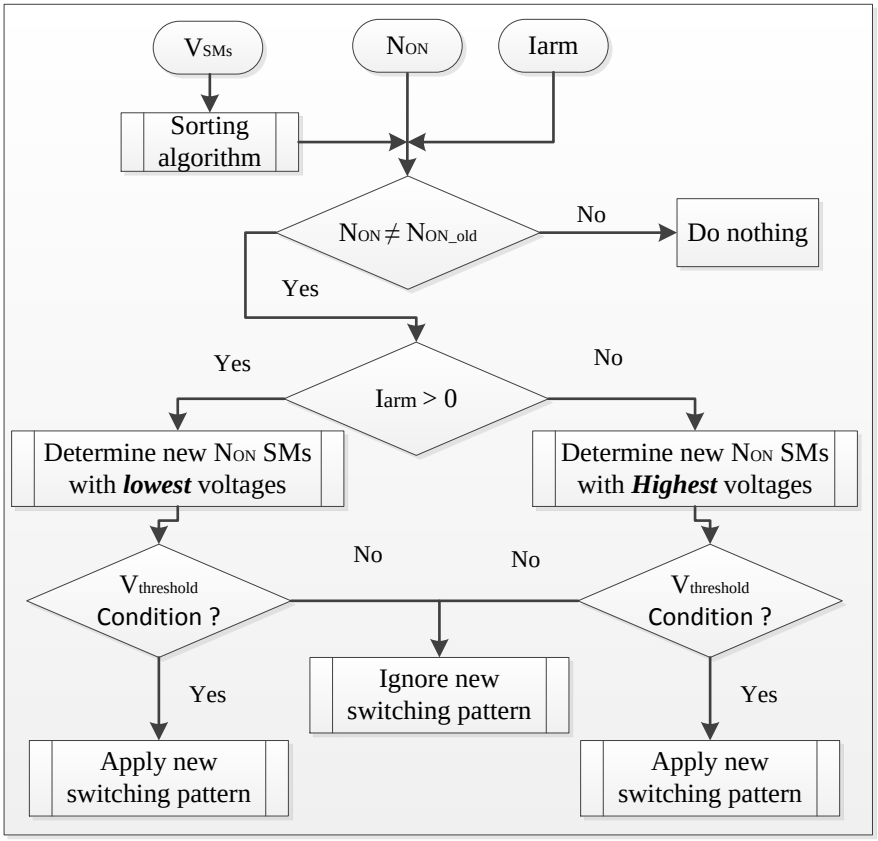

Figure 2.13 Voltage balancing algorithm with threshold

2.8.3 MinMax Algorithm

Figure 2.14 shows the flowchart of a voltage balancing algorithm that significantly reduces the switching losses [10]. The main difference of this algorithm compared to the previous ones is in the number of SM switching. It first checks if there is any change in N_{on} and then changes the switching state for just ΔN_{ON} SMs. For example if $\Delta N_{ON}=1$, it just inserts or bypasses one SM based on the arm current direction and keeps the switching state of the others SMs unchanged. If $\Delta N_{ON}>1$, it inserts or bypasses more SMs (equal to ΔN_{ON}) using the same approach.

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Therefore, the MinMax algorithm enjoys much lower switching of SMs resulting in much improved MMC efficiency. This of course comes with the cost of higher capacitor voltage ripple. In addition, the simulation results in PSCAD reveal that MinMax method cannot properly achieve voltage balancing if the number of SMs is higher than 20).

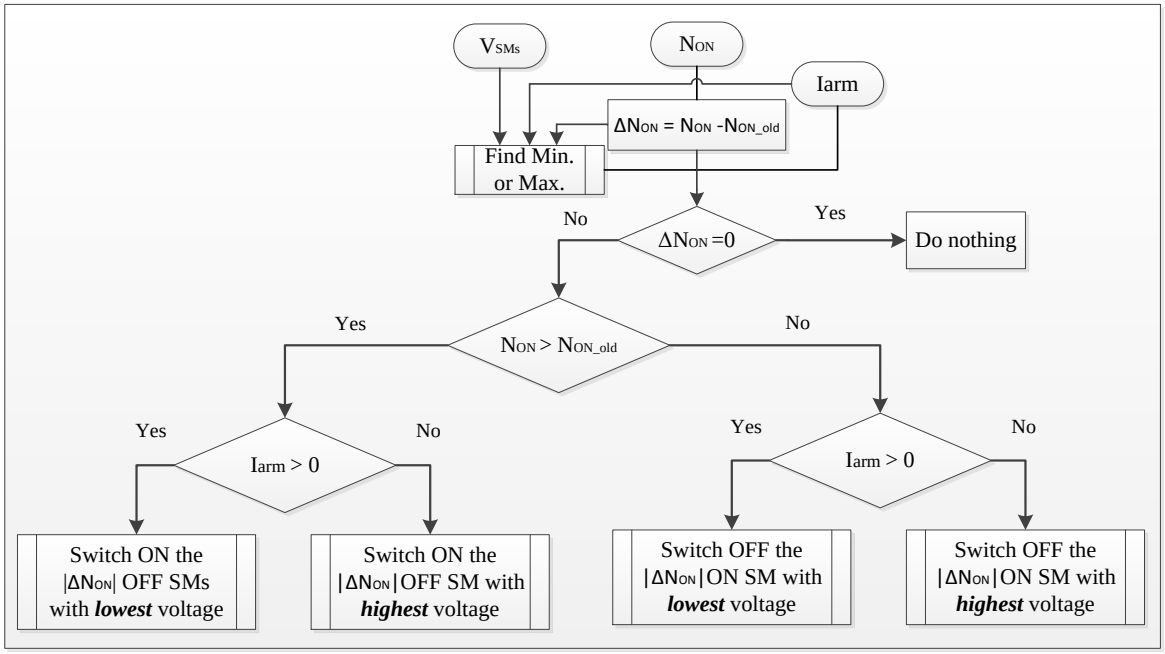

Figure 2.14 MinMax voltage balancing algorithm

Another important advantage of MinMax algorithm is that there is no need to apply full sorting algorithm and a simple method for finding minimum or maximum element of an array can be used instead. This significantly lowers processing burden which is very important in the processing hardware selection and cost.

2.8.4 Combined algorithm

One practical method is combining the MinMax algorithm with sorting algorithm as shown in Figure 2.15 [11]. This combined algorithm enjoys partially the benefits of low switching losses of MinMax algorithm and provides acceptable SMs voltages ripple. It can be summarized as follows:

- Execute the MinMax algorithm whenever ΔN_{ON} is changed, and
- Execute the full sorting algorithm for a number of times, $N_{rot,}$ in each cycle, which is called as cell rotation.

It is evident that more cell rotation (larger N_{rot}) will improve the SMs capacitor voltages ripple with the cost of increased the switching losses. Therefore, the suitable N_{rot} is the number of cell rotation that gives an acceptable ripple on the SMs capacitor voltage and the minimum switching losses.

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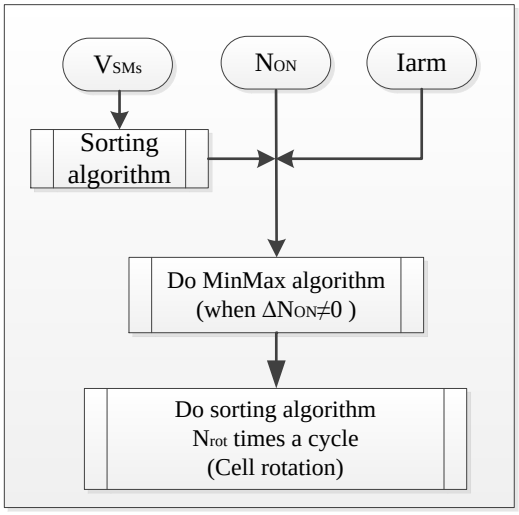

Figure 2.15 Combined voltage balancing algorithm

It should be noted that the cell rotation can be done at constant intervals over a cycle (as reported in [11]) or at slightly different intervals to be matched with the time when N_{ON} is changed. The simulation results on PSCAD show that the first case with constant intervals gives more power losses and slightly less ripple on the SMs capacitor voltage compared to the second case.

Example 2.3:

*Consider a 9-level MMC. The N_{ON} is changed 2*8=16 times a cycle as shown in Figure 2.10. Therefore, the MinMax algorithm is executed 16 times. If for example the number of cell rotation is considered N_{rot}=4, the sorting algorithm will run 4 times a cycle. For a case with constant intervals, the cell rotation is applied at the times t=0, T/4, T/2, 3T/4 where T is the period of reference voltage. Alternatively the cell rotation can be applied for specific values of N_{ON} say N_{ON}= 0, 4, 8, 12 and exactly when* ΔN_{ON} is changed*. It is understood that the first case has more changes in switching states of the SMs and therefore the switching losses are higher.*

Although implementing the cell rotation for the both above cases is easy to implement, the simulation results indicate that the performance will be better if the sorting algorithm runs at different distributed intervals according to the magnitude of I_{arm}. To implement this, we have determined three zones based on I_{arm} as described below:

1. **I_{arm} is very low;** in the interval when the arm current crosses zero the sign of I_{arm} will be changed. The sign changing event has significant impact on the selection of the SMs, since the highest or lowest SMs are selected based on direction of arm current. Without cell rotation in this range, the highest voltage SMs when I_{arm} becomes positive (or the lowest voltage SMs when I_{arm} becomes negative) will be kept ON which results in larger deviation in the SMs capacitor voltages. It should be noted that since I_{arm} is very small, the switching losses associated to cell rotation are negligible, and it is recommended to run sorting algorithm more frequently.
2. **I_{arm} is medium**; the sorting algorithm should be run at lower frequency.
3. **I_{arm} is very high**; although switching losses are high in this case, the cell rotation should be executed more frequently because high I_{arm} changes SMs voltage level very fast.

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This modified algorithm has been implemented by defining a parameter N_S and assigning different values to it for the above three zones. In this way, the sorting algorithm is executed when N_{ON} is a multiple of Ns; i.e. $N_{ON} = N_S, 2N_S, 3N_S$, etc. Ns should be a positive integer number.

For example, the following values of N_S may be used for a 21-level MMC:

1. If abs(Iarm)<0.1kA ➔ N_S =1; which means do the cell rotation every time N_{ON} is changed
2. if 0.1kA<abs(Iarm)<1kA ➔ N_S =10; which means do the cell rotation when N_{ON} =10 & 20
3. If abs(Iarm)>1kA ➔ N_S =4; which means do the cell rotation when N_{ON} =4, 8, 12, 16 & 20

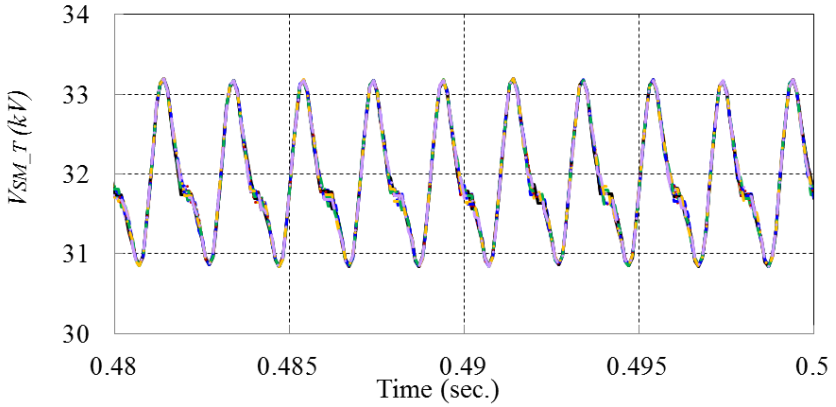
The optimum value for N_S in each zone is a variable that can be determined in simulation environment considering the criteria of switching losses and SMs capacitors voltage ripple.

2.8.5 Comparison of the algorithms

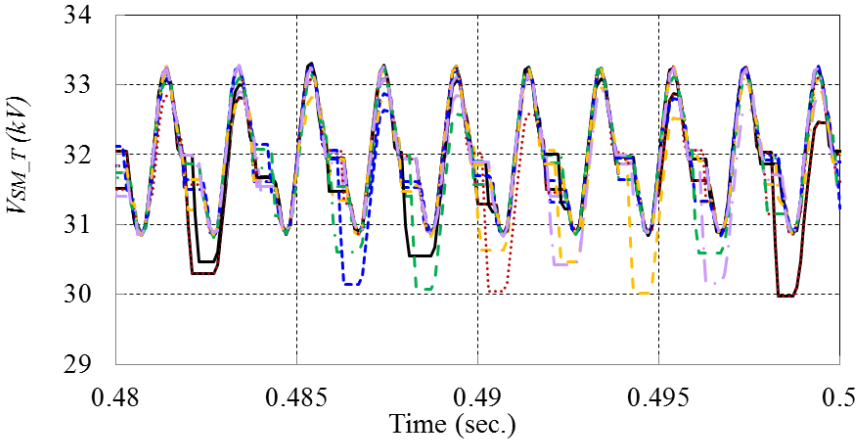
The voltage balancing algorithms can be compared based on two main criteria; 1) the switching losses, and 2) the SMs capacitors voltage ripple. Generally, the voltage balancing algorithms with higher switching rates give higher switching losses and lower SMs voltages ripple and vice versa. Figure 2.16 shows the voltage ripple for 4 selected algorithms obtained on MMC converter model of Figure 4.1 on PSCAD. The simulation conditions are kept identical for all cases; 3-phase, 21-level, 1000MVA MMC with same simulation time step, SM capacitance of 100uF, arm inductance of 5mH and operating frequency of 500Hz. It is seen that the basic sorting algorithm (Figure 2.16a) gives best capacitor voltage balancing while the MinMax algorithm (Figure 2.16c) gives the highest ripple and worst distribution of the SMs capacitor voltages. The sorting algorithms with changed N_{ON} (Figure 2.16b) and Combined algorithm (Figure 2.16d) show similar SMs voltages ripple. The switching losses for these four algorithms are calculated as 79.4MW, 45.2MW, 8.8MW and 24.5MW, respectively. The switching losses have been obtained based on the energy losses calculation of IGBT modules in PSCAD. This is discussed later in section 2.10.3 .

It is interesting to observe that the figures (b) and (d) have almost similar ripple with significantly different power losses. The reason is that the sorting algorithm with changed N_{ON} do much more execution of sorting algorithm compared to the combined algorithm, even if the SMs capacitors voltage levels are very close together. Therefore, the ripple improvement is negligible, but the power losses will increase significantly.

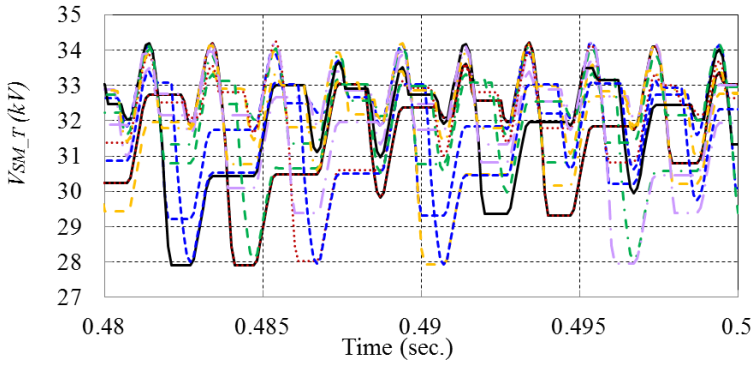
It can be concluded that the first two sorting algorithms (Figure 2.16a & Figure 2.16b) are not acceptable due to their large switching losses. The Combined algorithm gives better SMs capacitor voltage ripple but the MinMax algorithm gives significantly lower switching losses. It should be noted that although the switching losses of the combined algorithm is still high, it can be reduced by increasing the SM capacitance size and tuning the algorithm. The SMs capacitors voltage ripple of the MinMax algorithm can be also improved by increasing the SM capacitance size and modifying the algorithm as will be explained later in this report.



a) Basic sorting algorithm (SW_loss = 79.4MW)



b) Sorting algorithm with changed N_{ON} (SW_loss = 45.2MW)



c) MinMax algorithm (SW_loss = 8.8MW)

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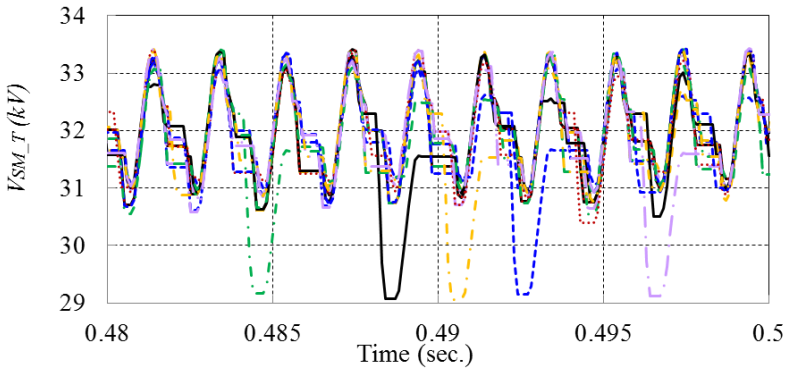

d) Combined algorithm (SW_loss = 24.5MW)

Figure 2.16 Comparison of SMs voltage ripple for 4 voltage balancing algorithms; a) Basic sorting algorithm, b) Sorting algorithm with changed N_{ON}, c) MinMax algorithm, d) Combined algorithm

2.9 Processing Resources

MMC arm control requires fast processing resources. At every execution time step, the SMs capacitors voltage levels and arm currents must be measured and converted to digital signals, and the modulation technique with voltage balancing algorithm must be executed. The duration of the execution time step should be lower than the minimum time between two consecutive N_{ON} changes (to not miss any $\Delta N_{ON} \neq 0$). From Figure 2.10, it can be seen that the time that N_{ON} is unchanged, T_K, is different depending on the magnitude of the input reference voltage. Therefore, the execution time step should be less than the minimum T_K. Considering an MMC with N_{cell} SMs per arm and operating at frequency f, a roughly estimate for the execution time step is $T_{exc}<1/(2*N_{cell}*f)$. Considering a conservative margin to avoid missing any change in Non, the execution time step may be selected half of the above time; i.e. $T_{exc}<1/(4*Ncell*f)$. For example for an MMC with N_{cell}=40 and f=500Hz, T_{exc}<12.5µs. This means that all the processing burden of this MMC should be done at a frequency of not less than 84kHz. This would be a tough task due to the size of the processing load.

A number of processing hardware options can be considered for this application. The two most common candidates are FPGA and TMS microcontroller. In this project an existing off the shelf board from national instrument (NI) is employed to implement the algorithms in a real time environment. This would give a realistic estimation of the maximum frequency the MMC code can be run. An image of this FPGA single board-RIO is shown in Figure 2.17. The main features of this board are:

- Programmable by Lab view software
- Reconfigurable Xilinx Spartan-6 LX45 FPGA for custom timing and control
- 16 high-speed simultaneous analogue inputs
- 14 high-speed digital output lines for IGBT or MOSFET switching
- 24 general purpose input lines

Figure 2.17 NI-SBRIO GPIC board

Two algorithms have been implemented on this FPGA board using LabView software; 1) A bubble-sort algorithm [12] to sort (in ascending order) an arbitrary array, 2) An algorithm to find the minimum and maximum components of that array. Their on-board execution times for an arbitrary array with different size (which represents different number of cells of MMC) have been measured and given in Table 2.2. The execution time of each algorithm has been obtained using a specific LabView module to measure the on-board clock time. The on-board times at the start and end of the algorithm are measured and their difference is obtained which is the execution time of the algorithm. These times have been obtained with the FPGA on-board clock 40MHz. These times will be reduced if the FPGA on-board clock increases.

It is seen that sorting an array needs much more time than finding its minimum and maximum especially if the size of array is large. Additionally, the execution time of finding minimum and maximum is proportional to the array size while it is proportional to **square** of array size for sorting algorithm. Although different sorting algorithms are proposed and some of them are more suitable to be implemented on FPGA, their long execution time is still a challenge if high operating frequency and number of cells are employed.

It should be noted that the voltage balancing algorithms have not been implemented completely and just two main blocks of them (sorting and finding minimum/maximum) have been implemented to verify and compare their execution times. In addition, the required times for measuring analog inputs (the conversion time of ADCs) are not considered.

From Table 2.2, the required time for just sorting a 400 elements array is 20700 µs. But it is known that currently MMC with N_{cell}=400 and operating frequency of 50Hz is used in industry which means that all the voltage balancing algorithms run in less than 25 µs. This implies that this FPGA board is not suitable for implementing the voltage balancing algorithms when the number of cell is high and more powerful FPGAs and processing units must be used for these cases.

Considering one analog input for arm current and one for arm reference voltage, this FPGA board can be used for arm control of MMC with maximum number of SMs equal to 14.

Table 2.2 Execution time for bubble-sorting and finding Minimum/Maximum of an array

Size of array	Sorting time (μs)	Finding Min/Max time (μs)
4	2.5	0.6
10	14.6	1.4
14	28	1.9
20	56	2.65
50	327	6.4
100	1303	12.4
200	5200	23.5
400	20700	44.5

2.10 MMC power losses

The power losses of an MMC can be divided into three groups:

1) Arm inductor conduction losses
2) SM conduction losses
3) SM switching losses

The conduction losses in arm inductor can be obtained by using the arm inductor resistance and calculating the rms value of arm current. The arm resistance can be measured or estimated.

An estimation of the conduction and switching losses of MMC SMs can be obtained using the IGBT and diode ON state characteristics, energy losses curves, and arm current.

2.10.1 Arm inductor losses

The arm inductor is a high-power air core inductor. Here a practical approach in designing such an inductor is given [2]. Figure 2.18 shows the topology of an air core solenoid inductor. The inductance can be reasonably well estimated with the following formula:

$$L = 0.2\times10^{-6}\pi^2 a\frac{2a}{l_{th}}N^2K \tag{1.12}$$

where *N* is the total number of turns, and *K* is Nagaoka's constant.

$$K = \frac{1}{1+0.9\frac{a}{l_{th}}+0.32\frac{t}{a}+0.84\frac{t}{l_{th}}} \tag{1.13}$$

where all parameters are shown in Figure 2.18.

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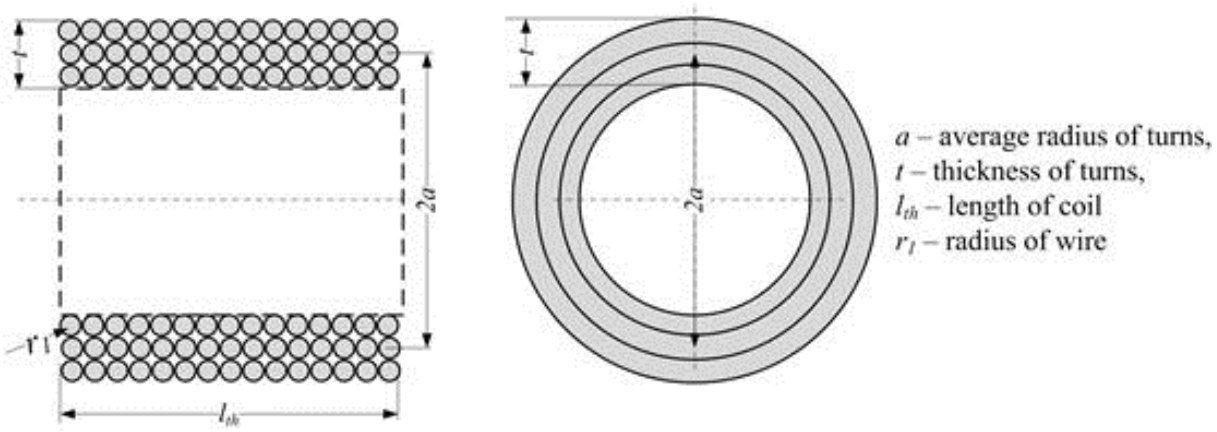

Figure 2.18 Solenoid air-core inductor [2]

The maximum value of L is obtained for 2a=3t. However this design option would imply densely wound coil, implying smallest surface for heat dissipation and likely high temperature of inner turns for high power designs. With high current designs the current density is usually taken as 1-4A/mm2 depending on the cooling arrangements. The cross section will be large and the wire is usually implemented using large number of stranded wires of smaller radius, or a series of rectangular wires similarly as with transformer designs. For high frequency applications (HF filters or DC/DC converters) Litz wire is used.

The total length of wire can be determined from the geometry of the solenoid and knowing the number of turns. Once length and wire cross section are known, the inductor resistance, mass and volume can be obtained using the cable specific resistance, and specific mass.

Example 2.4:

Design a 10mH arm inductor for 1000A MMC HVDC converter. Calculate total inductor mass, resistance and determine inductor loss assuming that copper wire is used. The density of copper is 8930kg/m3 and specific resistance is 1.73x10-8 Ω/m.

Solution

Assuming that current density is 2A/mm2, the conductor cross section and its radius will be 500mm^2 and r1=12.6mm. A 10% enamel insulation thickness is also assumed. Taking 7 layers and 13 turns in each layer gives N=91, l_{th}=0.361m, and with t=0.194m. Considering an average radius of turns a=0.5+t/2=0.597m, gives L=10.6mH.

The total length of wire is approximately 341m. The total mass is M_tot=1525kg, the total volume is V_tot=0.404m^3, and the total resistance is R_tot=0.0118Ω. Therefore at rated current the total arm inductor power loss is: P_{loss}=11.81kW. Considering 6 arm inductors for MMC, the total arm inductor power losses will be Ploss=71kW. It should be noted that the above resistance is calculated assuming low frequency current. If the operating frequency is higher, the resistance and power losses are higher because of skin effect. For example if the operating frequency is around 500Hz, it is good approximation to multiply the above resistance by 2.

2.10.2 SM conduction losses

The arm current passes through just one of the four components of a SM shown in Figure 2.2 at any time. Therefore, the conduction losses of a SM depend on the IGBTs and diodes conduction losses.

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An IGBT can be approximated with a series connection of threshold DC voltage source (u_{ce0}) representing IGBT on-state voltage with zero collector-emitter current and a collector-emitter on-state resistance (r_C). These two parameters can be obtained directly from IGBT datasheet as shown in Figure 2.19a [13]. It should be noted that the threshold voltage u_{ce0} and resistance r_C are obtained for two operating temperatures; one for T=25ºC and T=125ºC. Considering that the module works at average temperature of T=85ºC, the average value for the threshold voltage u_{ce0} and resistance r_C can be obtained by interpolation between these two values; i.e. 40% of T=25ºC plus 60% of T=125ºC.

The instantaneous conduction losses of IGBT and diode can be calculated as:

$$\begin{aligned} P_{cT}(t) &= \left(u_{CE0} + r_C \cdot i_{arm}(t)\right) \cdot i_{arm}(t) = u_{CE0} \cdot i_{arm}(t) + r_C \cdot i_{arm}^2(t) \\ P_{cD}(t) &= \left(u_{D0} + r_D \cdot i_{arm}(t)\right) \cdot i_{arm}(t) = u_{D0} \cdot i_{arm}(t) + r_D \cdot i_{arm}^2(t) \end{aligned} \tag{1.14}$$

The threshold voltage u_{D0} and resistance r_D can be obtained similarly as shown in Figure 2.19b.

Substituting the arm current with its DC and AC part:

$$\begin{aligned} P_{cT}(t) &= \left(u_{CE0} + r_C \cdot \left(i_{arm\_dc} + i_{arm\_ac}(t)\right)\right) \cdot \left(i_{arm\_dc} + i_{arm\_ac}(t)\right) \\ &= u_{CE0} \cdot i_{arm\_dc} + u_{CE0} \cdot i_{arm\_ac}(t) + 2r_C \cdot i_{arm\_dc} \cdot i_{arm\_ac}(t) + r_C \cdot i_{arm\_dc}^2 + r_C \cdot i_{arm\_ac}^2(t) \end{aligned} \tag{1.15}$$

By integrating the instantaneous power over one cycle and considering that the oscillatory terms have zero average over one period, the average conduction power losses are obtained as:

$$\begin{aligned} P_{cT\_ave} &= \int_0^T P_{cT}(t)dt \\ &= \int_0^T \left(u_{CE0} \cdot i_{arm\_dc} + r_C \cdot i_{arm\_dc}^2 + r_C \cdot i_{arm\_ac}^2(t)\right) dt \\ &= u_{CE0} \cdot I_{arm\_ave} + r_C \cdot I_{arm\_rms}^2 \end{aligned} \tag{1.16}$$

Where

$$\begin{aligned} I_{arm\_ave} &= i_{arm\_dc} \\ I_{arm\_rms}^2 &= i_{arm\_dc}^2 + i_{arm\_ac\_rms}^2 \end{aligned} \tag{1.17}$$

Similarly

$$P_{D\_ave} = u_{D0} \cdot I_{arm\_ave} + r_D \cdot I_{arm\_rms}^2 \tag{1.18}$$

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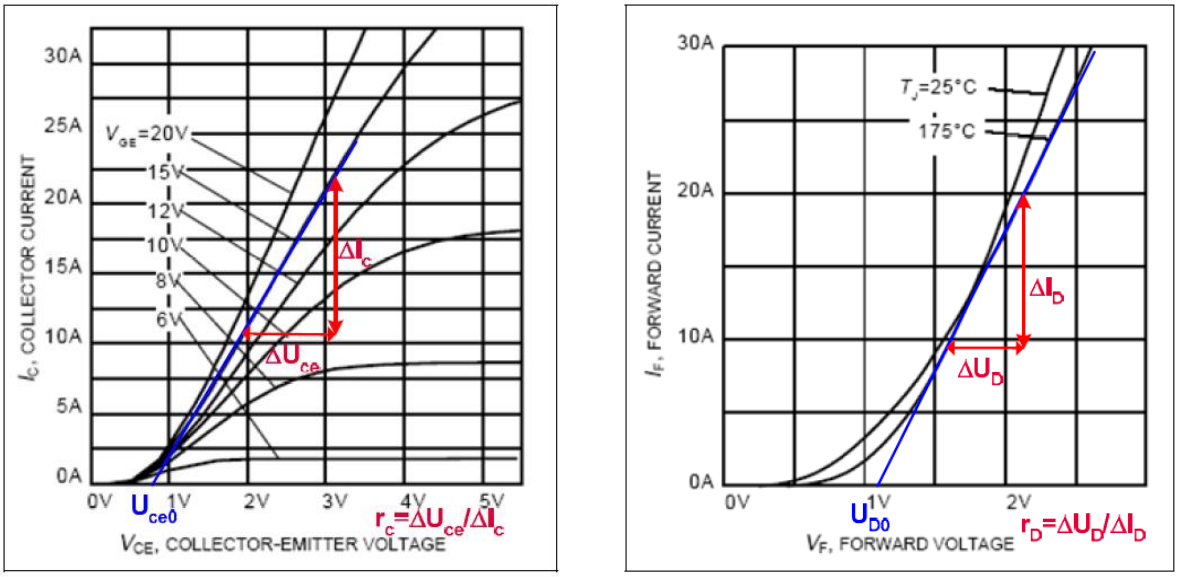

(a) (b)

Figure 2.19 Calculation of threshold voltage u_{ce0} and resistance r_C from on sate characteristics of IGBT and diode [13].

It should be noted that the calculation of the threshold voltages u_{ce0} and u_{D0} and resistances r_C and r_D shown in Figure 2.19 is only valid for a specific operating point. If we are calculating the instantaneous power losses, the threshold voltages and resistances should be calculated at any arm current. For the selected IGBT module ABB 5SNA 1300K450300, we obtained the following curve fitting exponential equations for the four parameters u_{ce0}, u_{D0}, r_C, and r_D using MATLAB:

$$\begin{aligned} u_{ce0}(t) &= 1.54 - 1.33e^{-2.3|i_{arm}(t)|} \\ r_C(t) &= 0.00116 + 0.0078e^{-14|i_{arm}(t)|} \\ u_{D0}(t) &= 1.73 - 1.31e^{-2.0|i_{arm}(t)|} \\ r_C(t) &= 0.00059 + 0.0078e^{-17|i_{arm}(t)|} \end{aligned} \tag{1.19}$$

The simulation results in PSCAD show that the instantaneous conduction losses are very close to the average conduction losses obtained using equations (1.16) and (1.18) with I_{arm_ave}=Idc/3=781A, I_{arm_rms}=920A, u_{ce0}≈1.38, u_{D0}≈1.52, r_C≈0.00116, and r_D≈0.00059.

2.10.3 SM switching losses

The switching losses of a typical SM are summation of the switching losses of its IGBTs and diodes. The switching losses of an IGBT and its freewheeling diode can be calculated using the typical switching energies diagrams which are given in the IGBT datasheet. Figure 2.20 shows IGBT switching ON and OFF (E_{on} & E_{off}) energies and diode reverse recovery energy (E_{rec}) for the ABB IGBT module 5SNA1300K450300 (4500V & 1300A).

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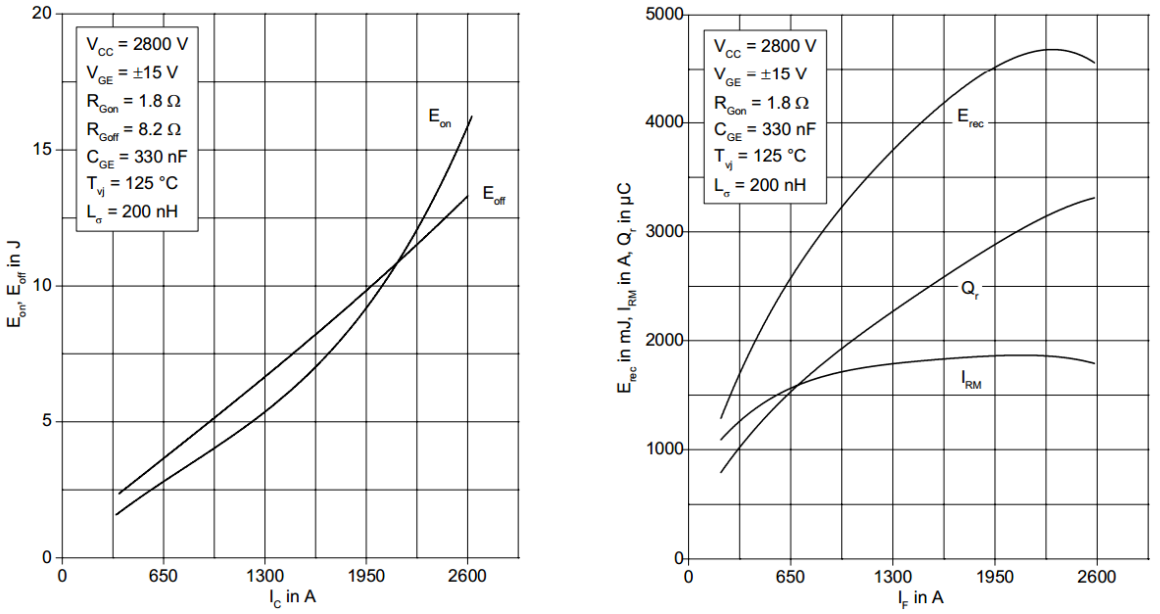

(a) (b)

Figure 2.20 ABB IGBT module 5SNA1300K450300 Switching energy diagrams for IGBT and diode or [14]

Some data sheets give the curve fitting equations for IGBT switching energy $E_{sw}=E_{on}+E_{off}$ and diode reverse recovery energy E_{rec} which are not given for this module. However, the given curve fitting equations are not accurate for small I_{arm} and in addition the IGBT switching equation is given for E_{sw} as sum of the ON and OFF switching losses and not for each of them separately. Therefore, we obtained the following curve fitting equations for E_{off}, E_{on} and E_{rec} for the selected IGBT module in order to use them in switching losses calculation.

$$\begin{aligned} E_{Off}(t) &= 0.277*\left|i_{arm}^3(t)\right| - 1.046*i_{arm}^2(t) + 5.97*\left|i_{arm}(t)\right| + 0.15 \\ E_{On}(t) &= 0.7552*\left|i_{arm}^3(t)\right| - 1.425*i_{arm}^2(t) + 4.663*\left|i_{arm}(t)\right| + 0.1 \\ E_{rec}(t) &= 0.2312*\left|i_{arm}^3(t)\right| - 1.78*i_{arm}^2(t) + 4.797*\left|i_{arm}(t)\right| + 0.13 \end{aligned} \quad (1.20)$$

Considering the four operating states of a SM (shown in Figure 2.2), it can be determined which components contribute to switching losses if a transition between these states occurs. Table 2.3 summarizes the switching losses contribution of the four components of a SM.

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Table 2.3 Switching losses contribution of the four components of a SM

	$I_{arm}>0$	$I_{arm}<0$
IGBT1: ↑ IGBT2: ↓	IGBT2 (sw_off)	IGBT1 (sw_on) D2 (sw_off)
IGBT1: ↓ IGBT2: ↑	IGBT2 (sw_on) D1 (sw_off)	IGBT1 (sw_off)

The switching energy for each of the four components IGBT1, IGBT2, D1 and D2 are calculated based on the equations (3.20) and Table 2.3. The switching energy of each SM is calculated by summation the energies of its four components and the switching power losses of one SM is the total switching energy in one second.

2.11 Design Summary

In this chapter we designed and fixed some of the MMC parameters and also presented appropriate equations that give a lower limit for SM capacitance and arm inductance. Table 2.4 summarizes this design results.

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Table 2.4 Design parameters of MMC bridge

SM type	Half-Bridge SM (See section 2.3)
Number of phases	3 (See section 2.4)
Number of levels	TBD
Operating frequency	TBD
SM capacitance	$C_{SM} > \frac{S_n}{8P * f * N_{cell} * V_{cell} * \Delta V_{cell}}$ (See section 2.5.1)
Arm inductance	$L_{arm\_res} > \approx \frac{0.1}{C_{arm}\omega^2}$ (See section 2.5.2)
IGBT module	ABB 5SNA1300K450300 (See section 2.5.3)
Modulation technique	NLM (See section 2.7
Voltage balancing algorithm	MinMax and combined algorithms (See section 2.8)
Processing resources	FPGA (ex. NI-RIO board) (See section 2.9)

In the next chapter, a range for the number of levels will be proposed. The parameters will be finalized in chapter 4.

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3. Harmonic Analysis of LCL DC-DC converter

Number of levels of MMC has significant impact on the generated voltage THD at its AC side. These harmonics deteriorate power quality and increase losses of the converter. For 2-level VSCs, large AC filters are usually used to avoid harmonic penetration to the AC grid. For MMCs, these harmonics can be highly mitigated by increasing the number of SMs.

In this chapter, harmonic analysis for a LCL DC-DC converter based on MMC will be studied. Note that the MMC application in DC/DC converter development is quite different from regular VSC applications as AC power quality is of lowest interest. The converter efficiency and operating frequency are the main converter parameters which are aimed to be as high as possible. To this reason, the objective is to find the minimum number of SMs for the MMCs to achieve an acceptable level of THD).

Figure 3.1 shows a schematic of a p-phase MMC based LCL DC-DC converter. It is composed of two MMC ports and one internal LCL circuit where the LCL comprises of two inductors L_{1x} and L_{2x}, and one capacitor C_x where subscript x represents the phase number. The voltage and current quality of the internal LCL circuit is not important and reducing the power losses is the main concern. In addition, its operating frequency can be selected according to design preferences. The detailed design of this LCL DC-DC converter and also its advantages and disadvantages against electrically-isolated (transformer-based) DC-DC converter will be given in the next phase of this project.

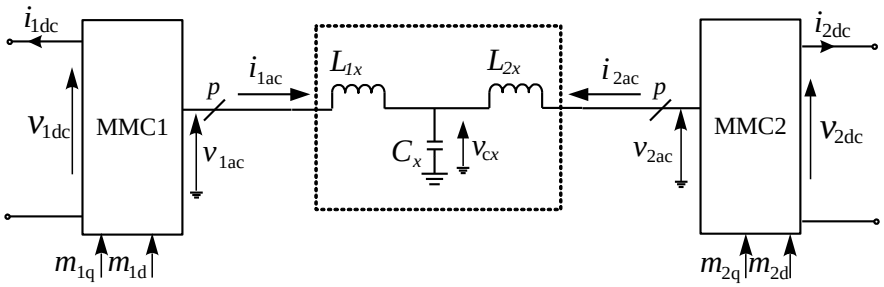

Figure 3.1 LCL DC-DC converter based on MMC

The MMC AC voltage is a staircase sinusoidal wave and it will be shown later that there are odd harmonics in the AC side voltages and currents. The magnitude of these harmonics depends on the number of levels (N_{cell}+1) of this staircase. It is evident that the MMC AC voltage v_{iac} becomes more sinusoidal by increasing the N_{cell} which results in lower harmonics in AC side and therefore lower losses within the internal LCL.

3.1 Voltage Harmonic Analysis

Assuming that the coordinate frame is linked with the AC capacitor voltage v_c, the MMC main harmonic of the AC voltage is given by:

$$v_{iac} = V_{iac}\sin(\omega t - \varphi_i), i = 1,2 \tag{2.1}$$

where V_{iac}, φ_i are the amplitude and phase angle of v_{iac}, and $\omega=2\pi f$ with f indicating the operating frequency of the internal circuit.

Figure 3.2 shows the phasor diagram of the DC/DC converter in a coordinate frame aligned with the capacitor voltage phasor. Note that both MMC ports are assumed working with PF=1 and hence the voltage and current on both sides are in phase.

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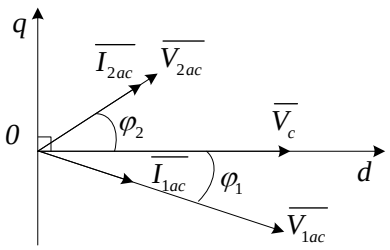

Figure 3.2 Phasor diagram of DC-DC converter voltages and currents

The AC voltages of MMC and internal capacitor C_x are shown in Figure 3.3 assuming a 9-level MMC bridge.

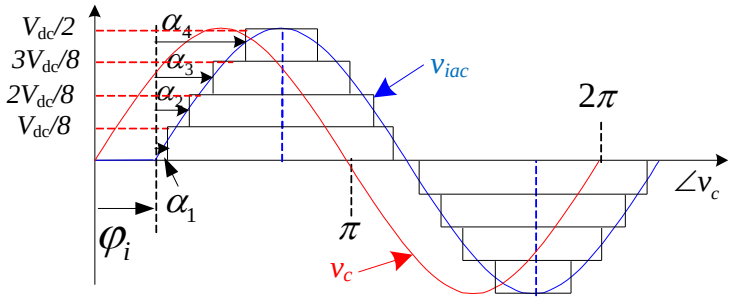

Figure 3.3 AC voltages of a 9-level MMC based LCL DC-DC converter

The AC voltage v_{iac} lags the capacitor voltage v_c with the angle φ_i. Using Fourier Series expansion and considering that the AC voltage is an odd function with respect to $\omega t=\varphi_i$, viac is:

$$v_{iac} = \sum_{n=odd} b_n \sin n(\omega t - \varphi_i) \tag{2.2}$$

Where b_n is (omitting index i):

$$b_n = \frac{2}{\pi}\sum_{k=1}^{N_{cell}/2}\int_{\alpha_k}^{\pi-\alpha_k}\frac{V_{dc}}{N_{cell}}\sin(n\omega t)\,d(\omega t)$$
$$b_n = \frac{2}{\pi}\sum_{k=1}^{N_{cell}/2}\frac{V_{dc}}{N_{cell}}\frac{2}{n}\cos n\alpha_k = \frac{4V_{dc}}{n\pi N_{cell}}\sum_{k=1}^{N_{cell}/2}\cos n\alpha_k \tag{2.3}$$

Therefore, the AC voltage is

$$v_{iac} = \frac{4V_{idc}}{\pi N_{cell}}\sum_{k=1}^{N_{cell}/2}\cos\alpha_k \sum_{n=1,3,5,\ldots}^{\infty}\left(\frac{1}{n}\sin n(\omega t-\varphi_i)\right)$$
$$= \frac{4V_{idc}}{\pi N_{cell}}\sum_{k=1}^{N_{cell}/2}\cos\alpha_k \sin(\omega t-\varphi_i) + \frac{4V_{idc}}{3\pi N_{cell}}\sum_{k=1}^{N_{cell}/2}\cos 3\alpha_k \sin 3(\omega t-\varphi_i) + \frac{4V_{idc}}{5\pi N_{cell}}\sum_{k=1}^{N_{cell}/2}\cos 5\alpha_k \sin 5(\omega t-\varphi_i)\ldots. \tag{2.4}$$

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The magnitude of the nth harmonic voltage relative to the fundamental is

$$\frac{v_{iac\_nth}}{v_{iac1}} = \frac{\left(\sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right)/n}{\sum_{k=1}^{N_{cell}/2} \cos \alpha_k} \tag{2.5}$$

The AC voltage total harmonic distortion THD_V is

$$THD_V = \frac{\sqrt{\sum_{n=3,5,7,\ldots} \left|V_{iac\_n^{th}}\right|^2}}{\left|V_{iac1}\right|} == \frac{\sqrt{\sum_{n=3,5,7,\ldots} \left|\frac{4V_{idc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right|^2}}{\left|\frac{4V_{idc}}{\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos \alpha_k\right|} \tag{2.6}$$

Figure 3.4 shows the ratio of 3rd, 5th and 7th harmonics and THD of the AC voltage with respect to the number of SMs. It is concluded that the THD of the AC voltage reduces below 1% when number of SMs is higher than 14.

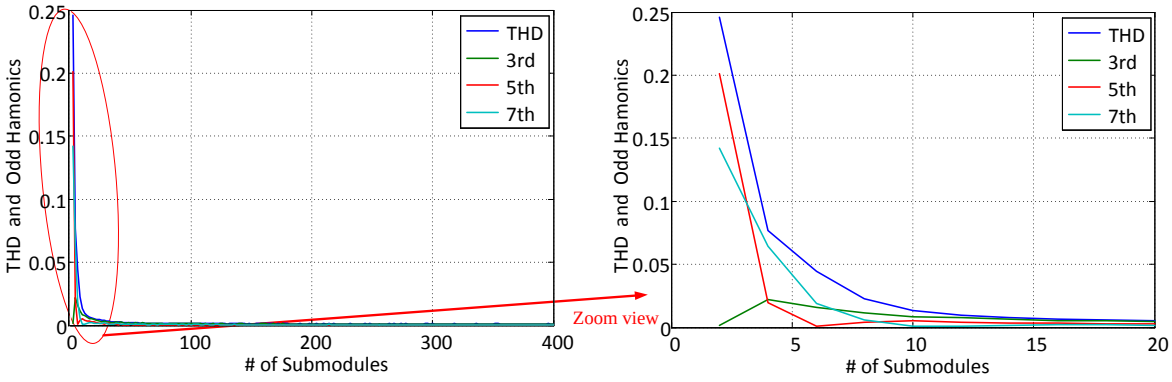

Figure 3.4 The relative magnitude of 3rd, 5th and 7th harmonics and THD of the converter AC voltage vs number of SMs

3.2 Current Harmonic Analysis

The magnitude and phase of the n[th] harmonic of the capacitor voltage, $v_{c\_n}{}^{th}$ is:

$$\left|v_{c\_n^{th}}\right| = \sqrt{\left(A\left|\frac{4V_{1dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right|\right)^2 + \left(B\left|\frac{4V_{2dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right|\right)^2 + 2AB\left|\frac{4V_{1dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right|\left|\frac{4V_{2dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right| \cos n\left(\varphi_1 - \varphi_2\right)}$$

$$\angle v_{c\_n^{th}} = \arctan\left(\frac{A\left|\frac{4V_{1dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right| \sin\left(n\varphi_1\right) + B\left|\frac{4V_{2dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right| \sin\left(n\varphi_2\right)}{A\left|\frac{4V_{1dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right| \cos\left(n\varphi_1\right) + B\left|\frac{4V_{2dc}}{n\pi N_{cell}} \sum_{k=1}^{N_{cell}/2} \cos n\alpha_k\right| \cos\left(n\varphi_2\right)}\right) \tag{2.7}$$

Where

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$$A = \frac{L_2}{L_1 + L_2 - L_1 L_2 C \omega_n^2}$$
$$B = \frac{L_1}{L_1 + L_2 - L_1 L_2 C \omega_n^2} \tag{2.8}$$

Therefore the magnitude of the n^{th} harmonic of the AC current i_{ac} is

$$\left|I_{iac\_n^{th}}\right| = \frac{\sqrt{\left|V_{iac\_n^{th}}\right|^2 + \left|V_{c\_n^{th}}\right|^2 - 2\left|V_{iac\_n^{th}}\right|\left|V_{c\_n^{th}}\right|\cos\left(\angle v_{iac\_n^{th}} - \angle v_{c\_n^{th}}\right)}}{L_i \omega_n} \tag{2.9}$$

Where $\omega_n=2\pi nf$. The ratio of the AC current n^{th} harmonic to the fundamental frequency component is

$$\frac{\left|I_{iac\_n^{th}}\right|}{\left|I_{iac1}\right|} = \frac{\sqrt{\left|V_{iac\_n^{th}}\right|^2 + \left|V_{c\_n^{th}}\right|^2 - 2\left|V_{iac\_n^{th}}\right|\left|V_{c\_n^{th}}\right|\cos\left(\angle v_{iac\_n^{th}} - \angle v_{c\_n^{th}}\right)}}{n\sqrt{\left|V_{iac\_main}\right|^2 + \left|V_{c\_main}\right|^2 - 2\left|V_{iac\_main}\right|\left|V_{c\_main}\right|\cos\left(\angle v_{iac\_main} - \angle v_{c\_main}\right)}} \tag{2.10}$$

The AC current THD_I is

$$THD_I = \frac{\sqrt{\sum_{n=3,5,7,\ldots}\left|I_{iac\_n^{th}}\right|^2}}{\left|I_{iac1}\right|} = \frac{\sqrt{\left|I_{iac\_3^{rd}}\right|^2 + \left|I_{iac\_5^{th}}\right|^2 + \left|I_{iac\_7^{th}}\right|^2 + \ldots}}{\left|I_{iac1}\right|} \tag{2.11}$$

An approximated ratio of 3rd, 5th and 7th current harmonics and THD of the AC current with respect to the number of SMs is shown in Figure 3.5. As expected, the harmonics and THD of the currents show similar behavior to the voltage harmonic study results shown in Figure 3.4. In addition, it is seen the ratio of the harmonics and also THD for current is smaller than the corresponding ones for voltage. This is a result of the attenuation of the higher order harmonics due to the impedance of the internal LCL circuit.

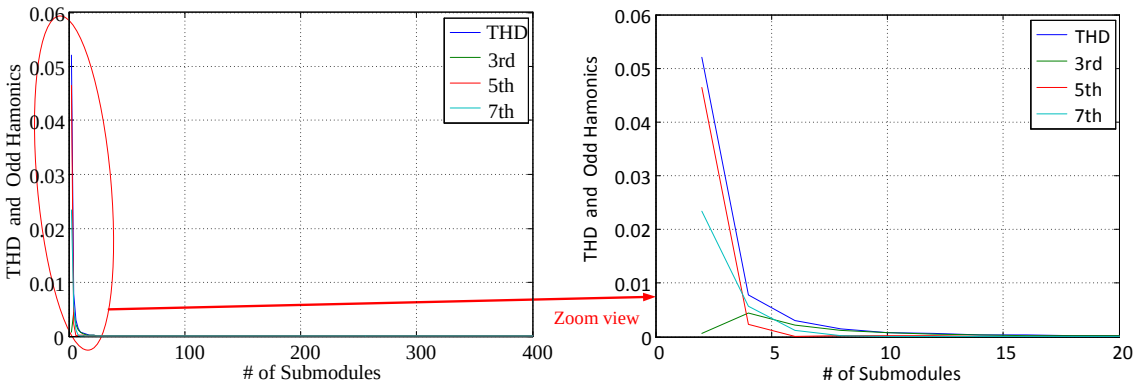

Figure 3.5 The ratio of 3rd, 5th and 7th harmonics and THD of the converter ac currents vs number of SMs

3.3 Discussion

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By examining at Figure 3.4 and Figure 3.5, it is seen that the harmonics content are decreased by increasing the number of SMs as expected. It also can be verified that the harmonics reduce below an acceptable level (1%) if the number of SMs is considered to above 12. However, the figures show saturation for higher number of cells which means that there is no significant improvement for higher number of cells. Therefore, this study recommends selecting MMC with more than 14 SMs per arm.

Selecting lower number of SMs brings benefits of simpler MMC capacitor voltage balancing with less switching (changes of IGBT states caused by balancing requirements) resulting in lower losses. On the downside, cell voltage becomes higher and more series-connected IGBTs per cell are required which brings voltage sharing challenges in series IGBT chains.

4. Simulation and final design

In this chapter, we will complete the design and finalize the following parameters:

- SM capacitance
- Arm inductance
- Voltage balancing algorithm
- Number of cells
- Operating frequency

The final design will be performed in PSCAD simulation environment and the impact of the above parameters on the SMs capacitor voltage ripple, power losses, cost, weight and volume of the converter will be investigated. The valves have been modeled based on their R_{ON} and R_{OFF} using FORTRAN coding in PSCAD with all cells represented as equivalent Thevenin circuit [17]. This modelling gives very good accuracy and running speed and also enables us to have different N_{cell}. Modeling MMC with high N_{cell} faces difficulties such as limitation on number of nodes and simulation burden time in PSCAD if accurate IGBT models are used.

In chapter 2, we have derived formula for minimum value of SM capacitance and arm inductance. However, as mentioned in section 2.5 , larger values are usually adopted in practical systems [11]. In section 4.2 , the best values for these two parameters will be determined based on simulation results and an approximate financial analysis.

The voltage balancing algorithms have been reviewed in section 2.8 and two of them (MinMax and combined algorithms) have been selected. In this chapter, the best voltage balancing algorithm will be selected and finalized considering the MMC power losses and SMs capacitors voltage ripple.

Number of cells has significant impact on harmonic content on AC and DC voltages and currents. In chapter3, we presented a harmonic analytical study on the AC voltage and current which verifies that MMC with minimum number of cells of 14 provides acceptable THD level for this application. In this chapter, the best number of cells will be investigated based on the power losses, SMs capacitors voltage ripple, AC and DC sides THD, and the required processing resource for implementation.

The operating frequency is the last parameter that will be finalized. It has significant impact on power losses, cost, weight and volume. The best operating frequency for offshore and onshore applications will be suggested.

4.1 Test system

Figure 4.1 shows the MMC bridge test system which is implemented in PSCAD. The MMC bridge is connected to a ±320kV DC supply through a transmission cable and a 3-phase 230kV AC grid. The DC cable model is considered in the test system to investigate the DC/DC converter harmonic injection effect to the DC system.

The transmission T-modelled DC cable data are R=0.095 Ω/km, L=2.1 mH/km, and C=0.21 μF/km [15]. The AC grid is composed of a 230kV, 1000MVA, 3-phase AC supply and a Y-Δ transformer (230/380, 1000MVA, 0.1pu) with SCR=10 and X/R=10.

The inner current control loops of the master control (see section 2.6) have been implemented with I_{dref}=1.0pu and I_{qref}=0.0 (to achieve full active power and zero reactive power at PCC). The CCSC has also been implemented based on the topology shown in Figure 2.6.

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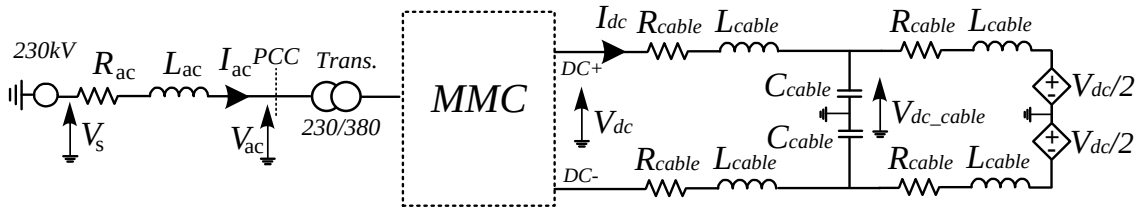

Figure 4.1 MMC bridge test system

Although we finalized some of the MMC parameters (SM type, number of phase and modulation technique) and limited the rest of them, there are still a high number of test cases if all possible combinations of the MMC parameters are considered at the same time.

Therefore, we try to reduce the number of test cases by fixing some of these design parameters and finding the best value for the others. At first, we investigate the best values for SM capacitance and arm inductance keeping other parameters fixed. Then, the impact of two voltage balancing algorithms (MinMax and combined algorithms) will be investigated. From the results of this simulation study, we will finalize the best voltage balancing algorithm and the appropriate range for C_{SM} and L_{arm}. Eventually, we will determine the suitable number of SMs and optimum operating frequency.

4.2 Selection of C_{SM}, L_{arm} and voltage balancing algorithm

In this section, the effect of C_{SM} and L_{arm} on the SMs power losses (conduction and switching) for the developed 21 level 500Hz MMC test systemFigure 4.1 is studied. The test will be done using both the MinMax and combined voltage balancing algorithms.

It is expected that the power losses and also SMs capacitor voltage ripple will decrease by increasing the C_{SM} and L_{arm}. In addition, the combined algorithm should give higher losses and lower ripple for the same C_{SM} and L_{arm} compared to MinMax method. Using the obtained tests results and an roughly financial analysis, the C_{SM}, L_{arm} and voltage balancing algorithm will be finalized.

4.2.1 Test results with the combined voltage balancing algorithm

Table 4.1 summarizes the test results for the modelled MMC bridge test system with combined voltage balancing algorithm. The number of cell rotation is selected around 7-8 per cycle. Note that since the sorting algorithm runs based on the I_{arm} and not at constant interval, as explained in section 2.8.2 , the N_{rot} may slightly vary at different cycles.

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Table 4.1 Loss and ripple results for the modelled test MMC bridge (Ncell=20, freq.=500Hz and combined voltage balancing algorithm)

C_{SM} (µF)	L_{arm} (mH)	ΔV_{cell} (%)	SMs Switching Losses (MW)	SMs Conduction Losses (MW)	SMs total Losses (MW)	SMs total Losses (%)
80	3	9.7	17.91	2.85	20.76	2.08
	10	9.4	14.78	2.84	17.62	1.76
	15	9.5	13.85	2.85	16.7	1.67
100	3	7.6	17.72	2.84	20.56	2.06
	10	7.3	14.47	2.83	17.3	1.73
	15	7.5	13.79	2.83	16.62	1.66
150	3	5.0	17.6	2.84	20.44	2.04
	10	4.7	14.28	2.83	17.11	1.71
	15	4.9	13.79	2.83	16.62	1.66
200	3	3.9	17.31	2.84	20.15	2.02
	10	3.4	14.12	2.84	16.96	1.69
	15	4.0	13.78	2.83	16.61	1.66
300	3	3.0	17.1	2.83	19.93	1.99
	10	2.3	14.01	2.83	16.84	1.68
	15	2.8	13.76	2.83	16.59	1.66
500	3	1.6	16.86	2.84	19.7	1.97
	10	1.3	13.97	2.83	16.8	1.68
	15	1.5	13.76	2.83	16.59	1.66

Figure 4.2 shows the total SMs losses and SMs capacitors voltage ripple percentage (ΔV_{cell}) based on the data of Table 4.1.

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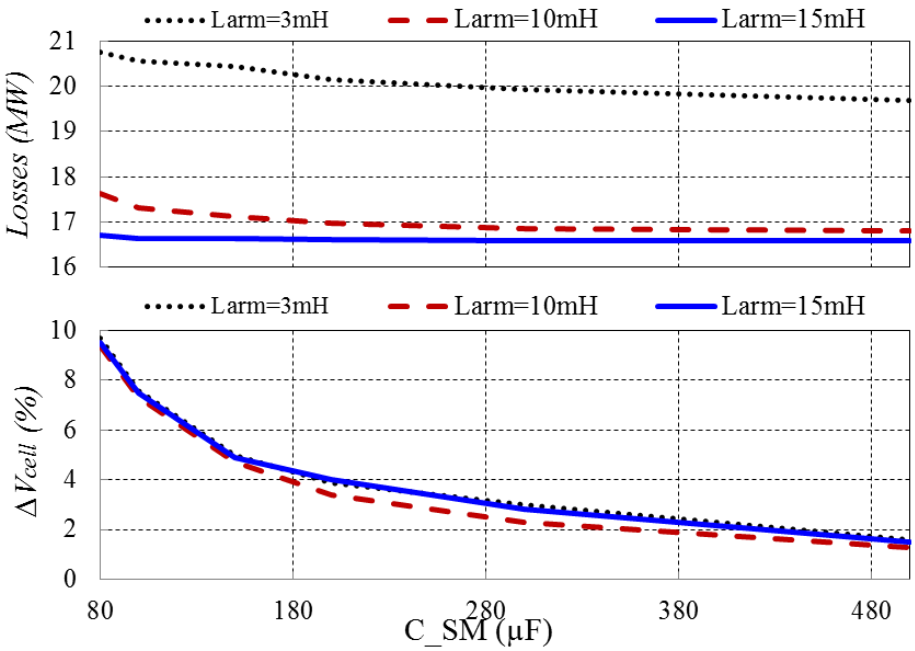

Figure 4.2 SMs power losses and voltages ripple percentage versus SM capacitance (Combined algorithm, Ncell=20, Freq=500Hz)

It is seen from Table 4.1 and Figure 4.2 that both the SMs power losses and voltages ripple are decreased by increasing the SM capacitance. It is also seen that these improvements will be saturated by further increase in SMs capacitance. This implies that there is an optimum SM capacitance that will be obtained later based on an approximate financial analysis.

Another important result is related to the effect of arm inductor. It is seen that for an identical SM capacitance, the power losses will be decreased by increasing the arm inductor. This effect is result of the ability of the arm inductance to improve the suppression of circulating current resulting in smoother the arm current. This will in turn reduce the voltage ripple and power losses. However, this improvement will be saturated by increasing the arm inductor larger than 15mH. In addition, it should be noted that the arm inductance cannot be increased too much because its inductive reactance at the operating frequency will become too high leading to the system instability. In aprticular, PSCAD simulations show that the system experiences instability if L_{arm} larger than 25mH is used. This is the reason that a maximum arm inductor of 15mH is adopted considering a safety margin from instability threshold.

Table 4.1 shows the test data just for C_{SM} >=80μF, because the SMs capacitor voltages ripple will go beyond 10% for lower C_{SM}. It is interesting to compare the results with previous theoretical analysis. Equation (3.6) gives C_{SM} >= 40μF for this converter to achieve voltage ripple less than 10%, but equation (3.6) gives the minimum appropriate SM capacitance considering an evenly dc voltage distribution amongst SMs is achieved. Since in practical applications, the voltage balancing algorithm runs at significantly lower rates (to reduce the losses and also for processing reasons), the SMs capacitance are usually selected higher.

Looking at the total SMs power losses in Table 4.1, it is seen that the SMs losses for one MMC at the best is 1.66%. Therefore, the losses for a DC-DC converter comprising of two MMC bridges and one internal LCL circuit (or internal transformer) will be above 3.5% which is not acceptable for high power DC applications.

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4.2.2 Test results with the MinMax voltage balancing algorithm

The power losses can be lowered either by decreasing the operating frequency or changing the voltage balancing algorithm. Here, we study the effect of voltage balancing algorithm on SMs power losses. We repeat the same MMC test system but MinMax voltage balancing algorithm is employed.

Table 4.2 summarizes the results obtained from the modelled MMC test system with MinMax voltage balancing algorithm.

Table 4.2 Loss and ripple results for the modelled test MMC bridge (N_{cell}=20, freq.=500Hz and MinMax voltage balancing algorithm)

C_{SM} (µF)	L_{arm} (mH)	ΔV_{cell} (%)	SMs Switching Losses (MW)	SMs Conduction Losses (MW)	SMs total Losses (MW)	SMs total Losses (%)
120	3	8.9	10.07	2.85	12.92	1.29
	10	8.7	7.56	2.84	10.4	1.04
	15	8.8	7.46	2.84	10.3	1.03
150	3	7.2	9.93	2.85	12.78	1.28
	10	6.9	7.54	2.85	10.39	1.04
	15	7.0	7.44	2.82	10.26	1.03
200	3	5.3	9.79	2.83	12.62	1.26
	10	5.2	7.52	2.83	10.35	1.04
	15	5.2	7.43	2.82	10.25	1.03
300	3	3.4	9.76	2.83	12.59	1.26
	10	3.3	7.51	2.83	10.34	1.03
	15	3.3	7.42	2.82	10.24	1.02
500	3	2.2	9.74	2.83	12.57	1.26
	10	2.1	7.51	2.83	10.34	1.03
	15	2.2	7.41	2.82	10.23	1.02

Figure 4.3 shows the magnitude of the total SMs losses and SMs capacitor voltages ripple percentage (ΔV_{cell}) versus C_{SM} based on the data of Table 4.2.

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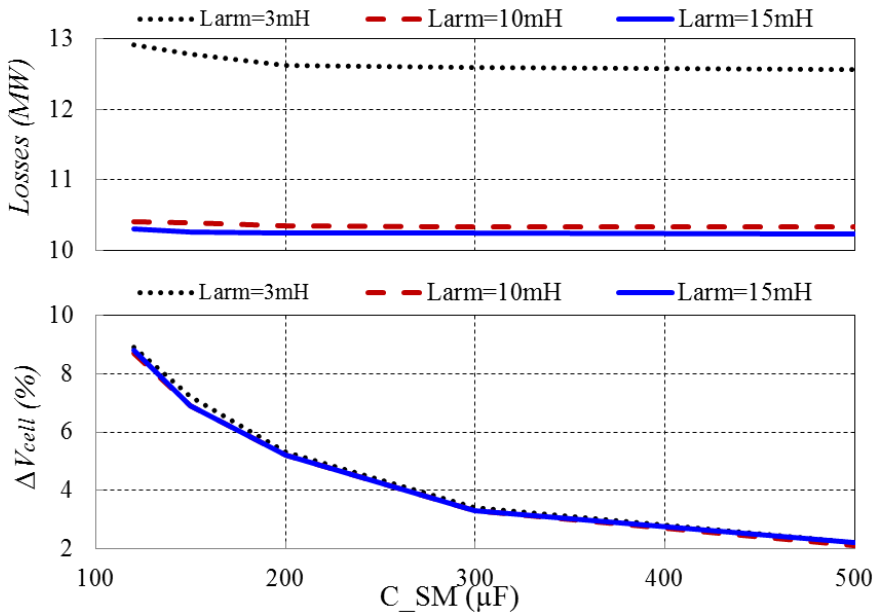

Figure 4.3 SMs power losses and voltages ripple versus SM capacitance (N_{cell}=20, freq.=500Hz, MinMax algorithm)

The results of Table 4.2 and Figure 4.3 show a similar performance; i.e. decreasing both the SMs power losses and capacitors voltage ripple by increasing the SM capacitance and/or arm inductance. This confirms the effect of SM capacitance and arm inductance on the SMs power losses and voltages ripple.

It is seen that the SM power losses reduce below 1.15% for one MMC bridge which implies that the losses for a DC-DC converter comprising of two MMC bridges and one internal LCL circuit (or transformer) will stay below 2.5%, which is reasonably acceptable for HVDC systems.

Note that a minimum cell capacitor of 120μF is used to achieve maximum 10% voltage ripple. This is a consequence of using MinMax voltage balancing algorithm which aims to improve converter efficiency by sacrificing on SM capacitor voltage ripple. However, the voltage ripple can be further reduced by increasing SMs capacitance as can be seen from Figure 4.3.

By comparing the results of the two voltage balancing algorithms, it can be concluded that the MinMax algorithm gives significantly lower losses with acceptable voltages ripple if larger SMs capacitors are adopted.

In the next section, an approximate financial analysis is presented with the aim of finding the relation between financial cost of the SMs capacitors and power losses. This will provide additional guideline to select the optimum voltage balancing algorithm and SM capacitance.

4.2.3 Financial analysis for SM capacitance selection

Every 0.1% losses for the studied 1000MW MMC is equal to 1MWh energy losses per hour or equivalently an annual energy loss of 8760MWh. Considering an average cost of energy around 1MWh ≈ €40 ≈ £30 [19], the cost of 0.1% losses for a 1000MW MMC would be £262,800 per year.

The cost of SMs capacitors for a 21-level, 640kV 1000MW MMC considering cell capacitance of 100uF, is roughly estimated. It is difficult to get accurate costs, but it is assumed that a 3000μF, 800V capacitor (with part number FFLI6B3007K) costs around $350 ≈ £232 .An arrangement of 80 in series

and 3 in parallel gives a 112μF, 64kV capacitor bank (considering a voltage safety factor of 2) which costs around £55680. Considering 20 SMs per arm, the total cost for the SMs capacitors of a 3-phase 1000MW MMC will be around £6.68m.

Although a 1000MW MMC converter is expected to work around 30 years, the lifetime of the capacitors are indicated between 50,000-100,000 hours depending on the temperature [18] which means they have an average lifetime of 10 years. Therefore, the capacitors cost is approximately equal to the cost of 0.25% power losses at 10 years.

It can be summarized that every 112μF, 64kV capacitor bank is roughly equal to the cost of 0.25% of losses. This means that if increasing the SMs capacitor by 112μF reduces the losses more than 0.25%, it is worth to select higher capacitors. This definitely verifies that MinMax algorithm with larger SMs capacitors gives more financial benefits. In addition, it is seen from Table 4.2 that for SMs capacitors higher than 150μF, the power losses reduction is not more than 0.25%, which means that it is not worth selecting larger SM capacitor. Therefore, we select C_{SM} =150μF which gives reasonable good SMs voltages ripple and power losses.

4.2.4 Arm inductance selection

From Table 4.2, it is seen that the modeled MMC SMs power losses with C_{SM} =150μF and L_{arm}=15mH is 0.13MW lower than the case with C_{SM} =150μF and L_{arm}=10mH.

From section 2.10.1 , the power losses for arm inductors of a 3-phase 1000MW MMC can be obtained. The power losses of six 10mH air core inductors with arm current 920A and current density 2A/mm^2 are estimated on 0.06MW for the 1000MW MMC. These losses for six 15mH inductors are obtained as 0.07MW.

Therefore increasing inductors has overall loss reduction, and we can easily select the highest applicable arm inductor of L_{arm}=15mH optimizing the converter loses and ensuring the MMC stability.

4.3 Selection of number of cells

In this section, we will investigate the effect of the number of cells and will provide the best value.

The number of cells has significant impact on the harmonics on both AC and DC sides of MMC. Lower number of cells increases the harmonics and THD, which worsens the power quality and increases the power losses. However, as discussed in chapter 3, the power loss is of main concern for DC-DC converter application and a number of cells as low as 14 would satisfy AC voltage quality.

In contrast, MMC with higher number of cells need more powerful and costly processing resources which will be challenging especially when the operating frequency is high. These two contradictory criteria imposed selection of the minimum number of cells that gives the THD less than an acceptable level. Reference [20] suggests the maximum THD of 3% on the DC voltages in DC grid.

Therefore, in this study, we measure the THD of the DC and AC signals, the SMs capacitors voltage ripple, and the power losses for different numbers of cells and evaluate the effect it would have on the suggested indexes. Table 4.3 summarizes the results for the modelled MMC bridge test system with operating frequency of 500Hz and L_{arm}=15mH.

It should be noted that the MinMax voltage balancing algorithm could not keep the SMs voltages balanced for all test cases (high number of cells). The voltage balancing algorithm for different N_{cell} is as follows:

- For N_{cell}=14 and 20, the MinMax voltage balancing algorithm has been used.

- For N_{cell}=30-100, the MinMax algorithm with an additional sorting algorithm has been used. Indeed, this is the combined algorithm with N_{rot}=1 and the cell rotation has been applied when N_{ON} is close to its minimum value.
- For N_{cell}=200 and 400, the combined voltage balancing algorithm with Nrot≈40 is employed to get the SMs voltage ripples less than 8%.

Table 4.3 Results for different N_{cell} (freq.=500Hz, L_{arm}=15mH)

N_{cell}	C_{SM} (µF)	Icir (p-p) (kA)	Iac (THD) (%)	Vac (THD) (%)	Idc (THD) (%)	Vdc (THD) (%)	Vdc_ cable (THD) (%)	ΔV_{cell} (%)	SM power losses (MW)	SM power losses (%)
14	105	0.06	0.88	1.1	0.18	0.22	0.2	6.7	10.28	1.03
20	150	0.045	0.6	0.7	0.15	0.16	0.1	7.0	10.27	1.03
30	225	0.035	0.25	0.4	0.1	0.13	0.05	6.2	10.77	1.08
40	300	0.03	0.25	0.4	0.06	0.13	0.04	6.5	10.46	1.05
50	375	0.028	0.22	0.4	0.05	0.09	0.02	7.9	10.22	1.02
100	750	0.02	0.22	0.3	0.05	0.08	0.02	7.4	10.26	1.03
200	1500	0.018	0.21	0.25	<0.01	0.03	<0.01	7.5	21.58	2.2
400	3000	0.01	0.21	0.25	<0.01	0.03	<0.01	7.7	21.52	2.2

From Table 4.3, it is concluded that:

- The circulating current is better suppressed by increasing N_{cell}. This is due to the fact that the active CCSC works better with higher resolution when N_{cell} increases.
- The THD of AC current decreases as N_{cell} increases. It is less than 0.9% for all cases and will be saturated around 0.2% by increasing further the N_{cell}. These THD are higher than the results of analytical study presented in chapter 4 because of different AC side (grid connected MMC) circuit and not evenly distributed capacitors voltages.
- The THD of AC voltage decreases as N_{cell} increases. It is less than 1.1% for all cases and will be saturated around 0.25% by increasing further the Ncell. This is in agreement with the results of analytical study in chapter 4.
- The THD of DC current is less than 0.18% for all cases. It is reduced by increasing N_{cell}l.
- The THD of DC voltages (at both the DC side of the MMC and the middle of the cable) are less than 0.22% for all cases. They are also reduced by increasing Ncell.
  Note: The THD of DC current and DC voltage depends also on the impedance of DC side; i.e. the length of DC cable. The reason is that the current source of the converter DC side is not an ideal current source especially for lower N_{cell}. It can be shown that the converter DC current becomes more ideal for higher Ncell. It can be also verified that the THD of DC current and voltage does not exceed 0.5% and 0.25% for any DC cable length.
- The SMs capacitors voltage ripples are similar for all cases. Actually, these similar voltage ripples have been achieved because of modification of the voltage balancing algorithm with the objective to keep the voltage ripple below 8%.
- The SMs power losses for N_{cell}=14 to N_{cell}=100 are similar. However, the power losses will be significantly increased for Ncell larger than 100. This is obviously due to the extra cell

rotations applied in SMs voltage balancing algorithm. In summary and considering all the above results, it can be recommended that the best number of cells is $20 \leq N_{cell} \leq 50$. It gives an acceptable level of harmonics on AC and DC currents and voltages and also low power losses. Note that we do not recommend minimum limit of 14 because this is the marginal N_{cell} obtained in section 3.3 . We also do not recommend higher N_{cell} due to extra power losses and processing burden it would cause. In addition, and based on the discussion in section 2.9 , the execution time step for $N_{cell} \geq 100$ and operating frequency 500Hz should be less than 10µsec which seems very challenging requirement.

N_{cell} equal to 20 is adopted to study the impact of operating frequency in the next section.

4.4 Selection of operating frequency

The operating frequency has immediate impact on the SMs switching losses, footprint size and weight of the converter's capacitors and arm inductors. By increasing the operating frequency:

- MMC switching losses increase.
- Size, weight and conduction losses of arm inductors decrease (provided that suitable Litz wire is used to mitigate skin and proximity effects).
- Size, weight and conduction losses of LCL inductors decrease (provided that suitable Litz wire is used to mitigate skin and proximity effects).
- Size and weight of SMs capacitors decrease.
- Size and weight of LCL capacitors decrease. The power losses of the capacitors are negligible.

In this section, the effect of operating frequency on the above items is investigated and the best operating frequency will be determined.

4.4.1 SMs power losses

Table 4.4 summarizes the SMs capacitors voltage ripples and power losses for operating frequencies in the range of 50Hz to 1000Hz. The number of SMs is fixed at $N_{cell}=20$ and the voltage balancing algorithm of MinMax is employed.

It is seen that the SMs capacitors voltage ripple increases slightly by increasing the operating frequency. This is because of higher SMs capacitance at lower frequencies which helps better SMs voltage regulation. This result implies that the SMs capacitance is not exactly proportional to the inverse of operating frequency as concluded in equation 2.7. However, the deviation is not too high and the equation is still valid for engineering applications.

The SMs power losses will be increased uniformly form 0.39% to 1.79% as the frequency increases from 50Hz to 1000Hz. Note that this increment is because of SMs switching losses while the SMs conduction losses are almost similar, as expected.

Table 4.4 SMs power losses for different operating frequencies (N_{cell}=20 and MinMax balancing algorithm)

Freq. (Hz)	C_{SM} (µF)	L_{arm} (mH)	ΔV_{SM} (%)	Switching Losses (MW)	Conduction Losses (MW)	Total Losses (MW)	Total Losses (%)
50	1500	50	6.5	1.07	2.84	3.93	0.39
100	750	30	6.4	1.83	2.84	4.67	0.47
200	375	25	6.8	2.99	2.84	5.83	0.58
300	250	20	6.9	4.47	2.83	7.3	0.73
400	190	15	7.0	5.97	2.83	8.8	0.88
500	150	15	7.0	7.44	2.83	10.27	1.03
600	120	15	7.3	8.84	2.82	11.66	1.17
700	107	10	7.2	10.47	2.82	13.29	1.33
800	94	10	7.3	11.86	2.83	14.69	1.47
1000	75	5	7.5	15.11	2.84	17.95	1.79

4.4.2 Arm inductors and SMs capacitors losses, weights and volumes

The arm inductors are considered as air core inductors with conductor rms current 920A and current density 2A/mm2. Detailed calculations of LCL inductor losses, weight and volume were given in section 2.10.1 .

The SMs capacitors losses are negligible compared to the inductor losses, and therefore are ignored in this report. The SM capacitors are DC voltage capacitors and their weight and volume can be estimated by arranging a number of smaller capacitors in series and parallel. For example, a number of 3000uF, 800V capacitors (with part number FFLI6B3007K) can be used to produce the SMs capacitors as mentioned in previous section. Considering that the size of one capacitor is around 3590cm^3 [18], the volume of one capacitor bank 112µF at 64kV will be around 1m^3 (considering 15% extra space).

The weight of one capacitor 3000µF at 800V is 4.5kg. Therefore the weight of one capacitor bank 112uF at 64kV will be around 1100kg. It should be noted that these calculations are approximate and just give an estimation of the weight and volume of the capacitor bank of the LCL converter.

Table 4.5 summarizes the results for the power losses, weight and volume of the arm inductors and SMs capacitors for a 3-phase MMC with N_{cell}=20.

Note: The weight and volume of the inductors are calculated based on an estimated average radius of turns, number of layers and number of turns in each layer (see section 2.10.1). It is possible to obtain different resistance, weight and volume for the same inductance by changing the above parameters of the inductor. Therefore, these values are approximated.

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Table 4.5 Power loss, weight and volume of arm inductors and SMs capacitors (N_{cell}=20)

Freq. (Hz)	C_{SM} (µF)	L_{arm} (mH)	R_L (mΩ)	Total L_{arm} power losses (MW)	Total weight (Ton) (6* L_{arm}+6*20* C_{SM})	Total volume (m^3) (6* L_{arm}+6*20* C_{SM})
50	1500	50	29	0.15	23.0+1768=1791	6.4+1607=1613
100	750	30	24	0.12	18.8+884=903	5.6+804=810
200	375	25	20	0.1	15.6+442=458	5.2+402=407
300	250	20	17	0.09	13.2+295=308	4.4+268=270
400	190	15	14	0.07	11.2+224=235	4.0+204=208
500	150	15	14	0.07	11.2+177=188	4.0+161=165
600	120	15	14	0.07	11.2+142=153	4.0+129=134
700	107	10	11	0.06	9.4+126=135	2.8+115=118
800	94	10	11	0.06	9.4+111=120	2.8+101=104
1000	75	5	7	0.04	5.6+88.5=94	1.6+80.3=82

4.4.3 LCL Inductors and capacitors losses, weight and volume

Each phase of the internal LCL circuit of DC-DC converter has 2 inductors and one capacitor as illustrated in Figure 4.1. Therefore, there are 6 inductors and 3 capacitors in a 3-phase LCL DC-DC converter. Table 4.6 shows the required inductors and capacitors calculated for a ±320kV (unity step ratio), 1000MW LCL DC-DC converter for different operating frequencies (the theory of LCL DC-DC converter and calculation of its parameters is given in [3] and will be analyzed in more depth in next phase of this project).

The power losses, weight and volume of the LCL inductors are calculated similar to the arm inductors. The only difference is that the rms current of each phase is around 1520A.

The LCL capacitors size is achieved using a similar approach used for MMC cell capacitors. A capacitor bank of 1µF and 520kV (considering voltage safety factor 1.5) can be achieved by an arrangement of series parallel connection of 4500 of 1100µF and 230V AC capacitors (with part number 947D112K102DLRSN-ND from [18]). Considering that the size of one capacitor is around 1700cm^3 [18], the volume of the 1µF 520kV capacitor bank of 1µF will be around 9m^3 (considering 20% extra space). The weight of the capacitor 1100µF and 230V is 1.8kg. Therefore the weight of the capacitor bank 1µF and 520kV will be around 8100kg. The LCL capacitors losses are neglected compared to the inductor losses.

Table 4.6 summarizes the power losses, weight and volume of LCL inductors and capacitors for a 3-phase LCL circuit for different frequencies.

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Table 4.6 Power losses, weights and volumes of the LCL inductors and capacitors

Freq. (Hz)	L_{LCL} (mH)	C_{LCL} (µF)	R_L (mΩ)	Total power losses (MW)	Total weight ($*10^3$kg) ($6* L_{LCL}+3* C_{LCL}$)	Total volume (m^3) ($6* L_{LCL}+3* C_{LCL}$)
50	530	12.0	84	1.16	166+292=458	59+320=379
100	265	6.0	55	0.77	110+146=256	36+160=196
200	132	3.0	36	0.5	72+73=145	19+80=99
300	88	2.0	28	0.39	56+49=105	15+54=69
400	66	1.5	24	0.34	54+37=91	14+40=54
500	53	1.2	21	0.29	42+29=71	11+32=43
600	44	1.0	19	0.26	37+25=62	10+27=37
700	38	0.85	17	0.24	34+21=55	9+23=32
800	33	0.75	16	0.22	31+18=49	8+20=28
1000	26	0.6	14	0.19	27+15=42	7+16=23

4.4.4 Total power losses, weight and volume of DC-DC converter

The LCL DC-DC comprises of two MMCs and one 3-phase LCL circuit. Therefore, the total power losses of LCL DC-DC converter include the MMC SMs power losses (switching and conduction losses) multiplied by 2, the arm inductors conduction losses multiplied by 2 and the internal LCL inductors conduction losses. The weight and volume study of LCL DC-DC converter includes just the components that have an impact with operating frequency; i.e. the SMs capacitors, arm inductors, LCL inductors and capacitors. Therefore, the total weight and volume are composed of the weight and volume of SMs capacitors and arm inductors for two MMCs, and the LCL inductors and capacitors.

Table 4.7 summarizes the total power losses, weight and volume of a LCL DC-DC converter for different operating frequency. Figure 4.4 illustrates the data of Table 4.7.

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Table 4.7 Total power losses, weight and volume for LCL DC-DC converter

Freq. (Hz)	Total Weight (*10^3 kg)	Total volume (m^3)	Total SMs power losses (MW)	LCL inductors conduction losses (MW)	Total L_{arm} conduction losses (MW)	Total power losses (MW)	Total power losses (%)
50	4040	3605	7.86	1.16	0.3	9.32	0.93
100	2062	1816	9.34	0.77	0.24	10.35	1.04
200	1061	913	11.66	0.5	0.2	12.36	1.24
300	721	619	14.6	0.39	0.18	15.17	1.52
400	561	470	17.6	0.34	0.14	18.08	1.81
500	447	373	20.54	0.29	0.14	20.97	2.1
600	368	350	23.32	0.26	0.14	23.72	2.37
700	325	268	26.58	0.24	0.14	26.94	2.69
800	289	236	29.38	0.22	0.12	29.72	2.97
1000	230	187	35.9	0.19	0.08	36.17	3.62

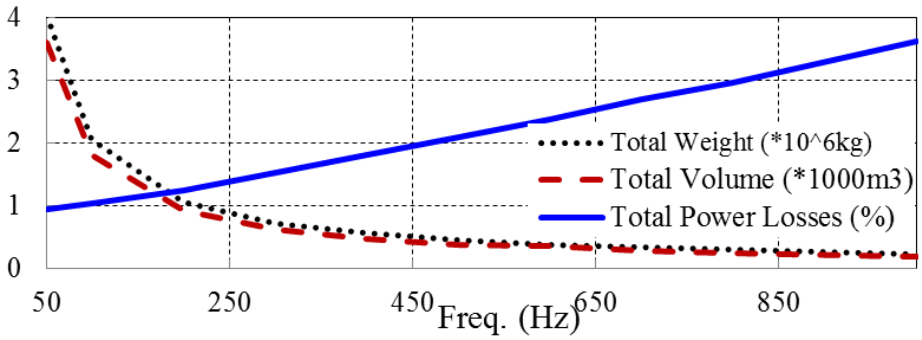

Figure 4.4 Total power losses, weight and volume for LCL DC-DC converter

It is seen that by increasing the operating frequency, the total power losses increase while the total weight and volume decrease. Although the total power losses for 50 and 100Hz are very low, the total weight and volume are very high. Therefore, the operating frequency below 200Hz is not acceptable.

Selection of the exact frequency is a tradeoff between the power losses and the cost of land and also the equipment for the corresponding volume and weight. For example, the power losses are more important for onshore applications while for offshore applications, the weight and volume have highest priority. Therefore, a suggestion for the suitable operating frequency can be:

- For onshore applications: 200Hz-400Hz (for example: 300Hz)
- For offshore applications: 400Hz-600Hz (for example: 500Hz)

Note: The skin effect has not been considered in the calculation of the inductors resistance and power losses. However, it can be shown that it has no significant effect on the final conclusion about the operating frequency range. For example, if all the inductors conduction losses are multiplied by an appropriate factor for skin effect (for example, 1.5 for freq.=200, 2 for freq.=500 and 3 for freq.=1000), the total power losses increase less than 3% which does not change the selected operating frequency.

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4.5 Design Summary

The final design results for the modeled MMC bridge for application in DC-DC converter are summarized in Table 4.8.

Table 4.8 Final design parameters of MMC bridge

SM type	Half-Bridge SM (See section 2.3)
Number of phases	3 (See section 2.4)
Number of levels	20 (See sections 2.4 3.3 & 4.3)
Operating frequency	300 Hz (See section 4.4)
SM capacitance	250μF (See sections 2.5.1 & 4.2)
Arm inductance	20mH (See section 2.5.2 & 4.2)
IGBT module	ABB 5SNA1300K450300 (See section 2.5.3)
Modulation technique	NLM (See section 2.7)
Voltage balancing algorithm	MinMax algorithms (See section 2.8)
Processing resources	FPGA (ex. NI-RIO board) (See section 2.9)

4.6 Test of designed MMC bridge

The performance of the MMC test system of Figure 4.1 with the final parameters of Table 4.8 has been verified on PSCAD for normal operation as well as a number of severe disturbances.

4.6.1 Power reference step

Figure 4.5 shows the results for a power reference step change from 1pu to -1pu at t=0.5sec. The results verify that the system is stable for this extreme power step.

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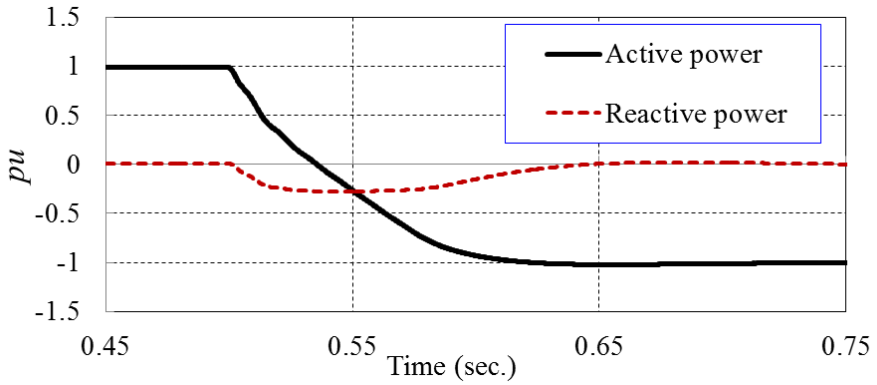
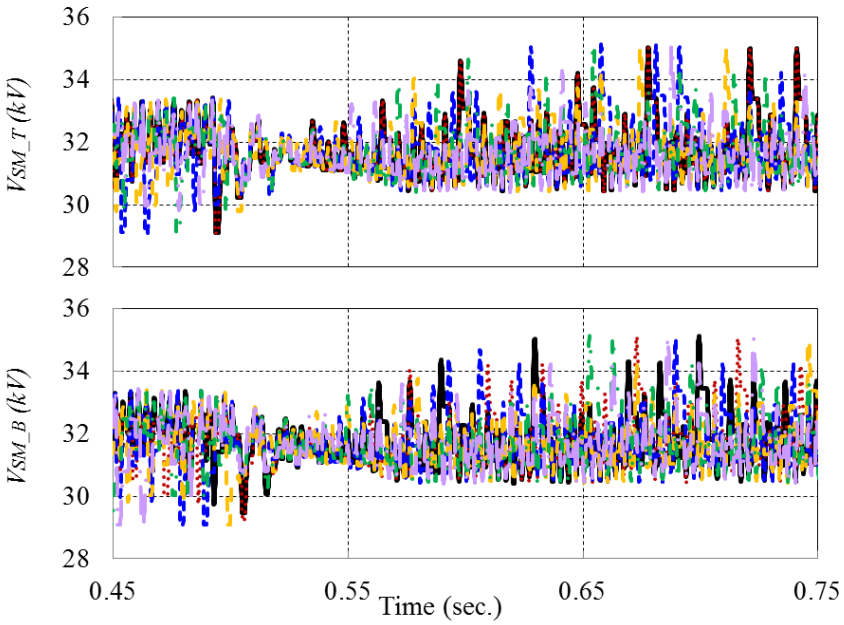


a) Active and reactive power



b) Upper and lower arms SMs capacitors voltage on one phase

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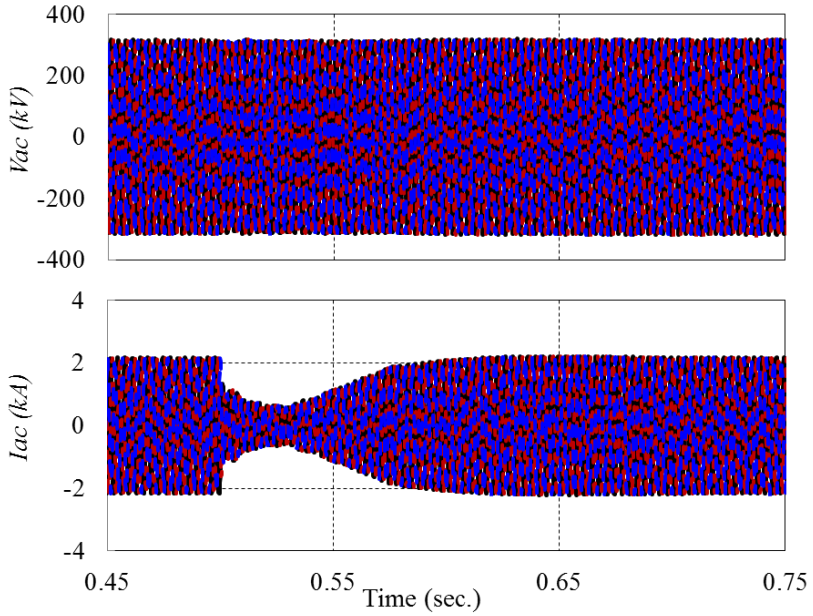
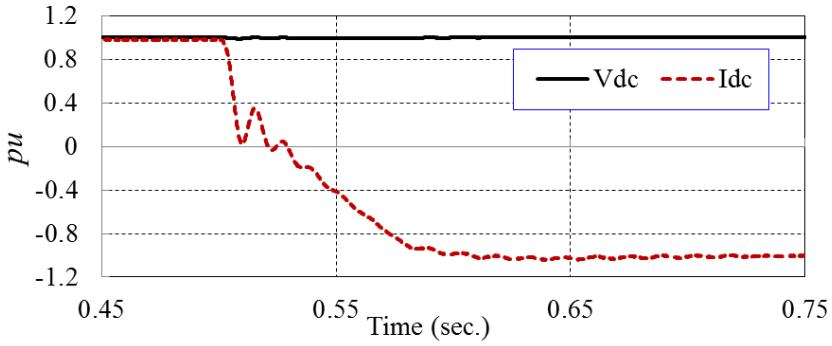


c) AC voltage and current



d) DC voltage and current

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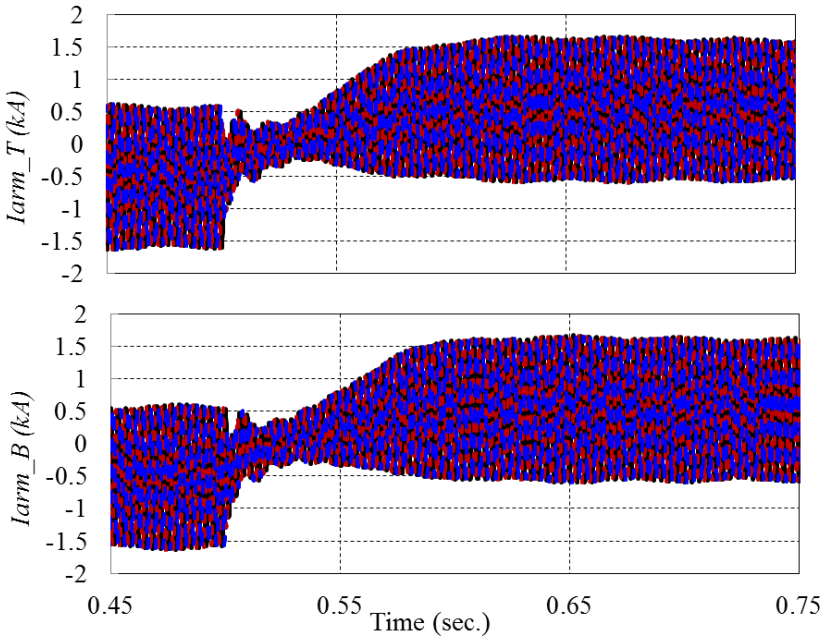
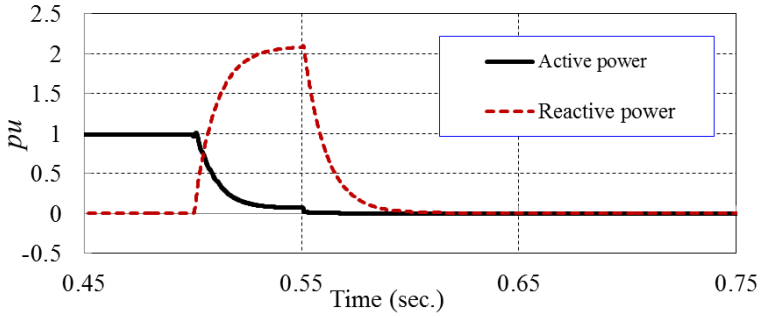


e) Upper and lower arm currents

Figure 4.5 Power reference step change response

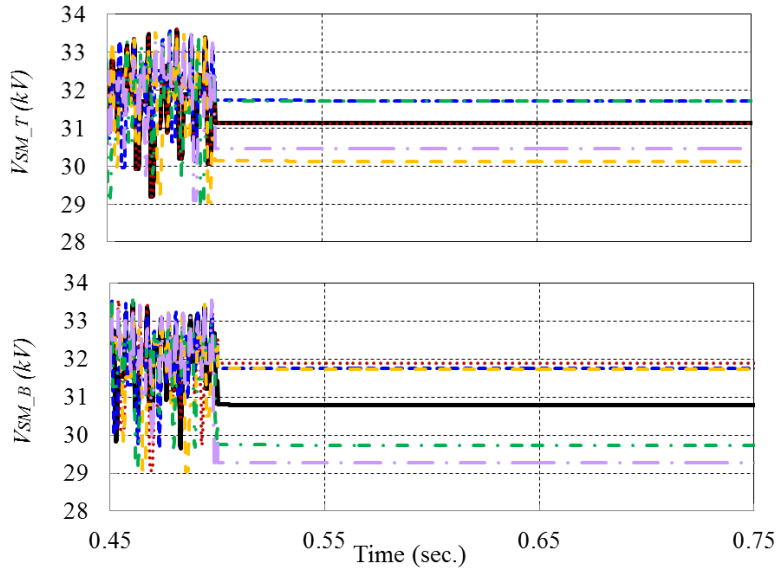
4.6.2 DC fault

Figure 4.6 shows the results of applying a permanent symmetrical DC fault at t=0.5sec. Immediately after the DC fault, the IGBTs are blocked, and after 50msec the AC circuit breaker is tripped. The results verify that the acceptable performance of the system. It is seen that the SMs voltages retain charged and do not discharge in the fault.

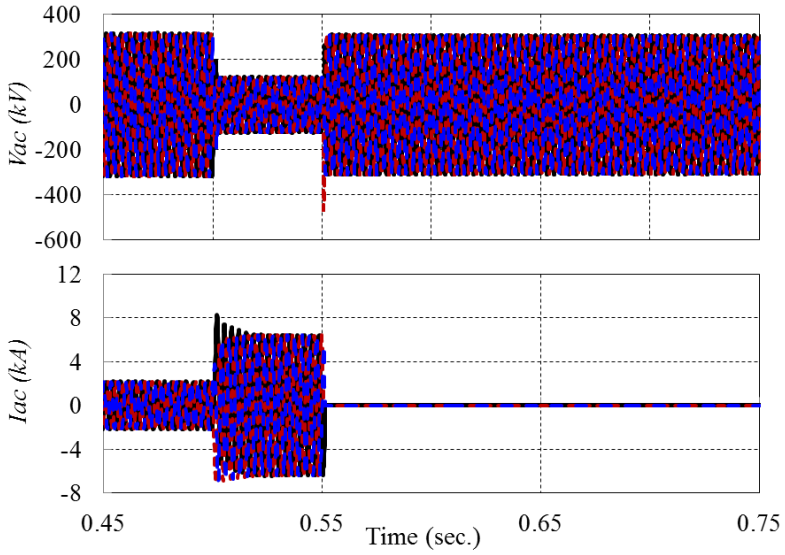


a) Active and reactive power

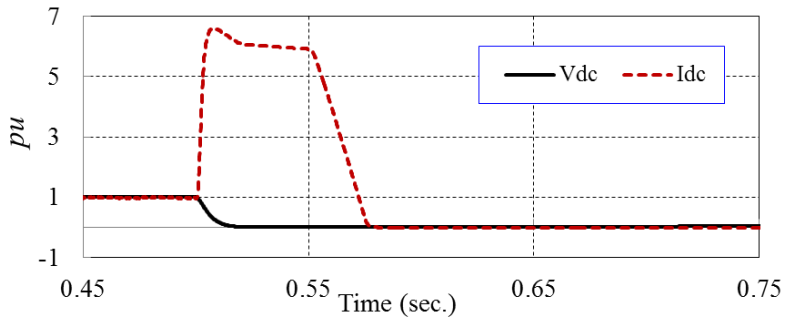
The National HVDC Centre



b) Upper and lower SMs capacitors voltage



c) AC voltage and current



d) DC voltage and current

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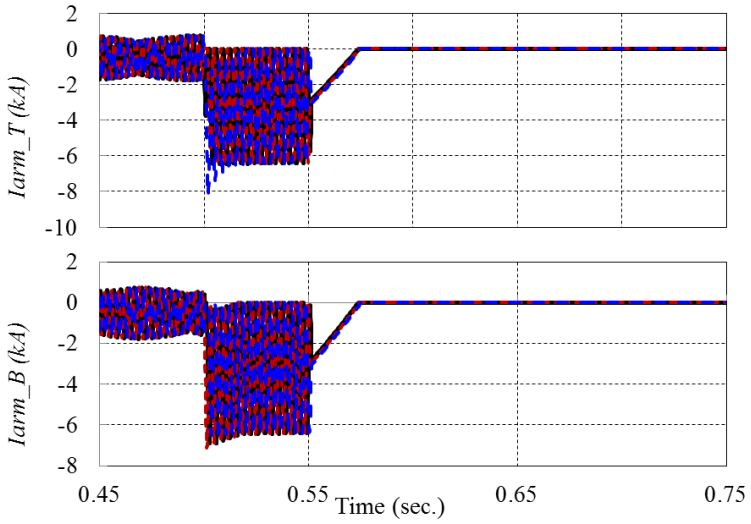

e) Upper and Lower arm current

Figure 4.6 DC fault response for the MMC test system with final parameters

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5. Conclusion

A 1000MVA, ±320kV, medium frequency MMC is studied and designed in this document. The MMC is intended to be used in high power DC-DC converters and DC hubs. These parameters analyzed include:

- SM type (Half-bridge or Full-bridge)
- Number of Phases
- IGBT switches
- Processing resources
- Modulation technique
- Arm inductance and capacitance
- Voltage balancing algorithms
- Number of levels
- Operating frequency

The analytical study of the cell capacitor size concluded that a detailed formula is required which explicitly involves operating frequency and cell voltage ripple. The study of arm inductor determined the analytical expression for inductance which avoids resonance with arm capacitor and enables low MMC losses.

The MMC cell voltage balancing algorithm is found to have impact on both voltage ripple and converter losses and therefore has been analyzed in depth. It is concluded that simple MinMax algorithm gives adequate voltage balancing when cell number is at most 20, while significantly reduces losses.

A full analytical study is completed to determine required number of cells in MMC. The harmonic analysis indicates that MMC should have at least 14 cells and that there is no significant benefit in using much higher number of cells. The number of cells is demonstrated to play key role in the switching losses, due to complications with voltage balancing algorithm. Additionally, it would increase processing burden of the MMC and will demand more powerful digital processing resources.

The initial theoretical conclusions are verified on detailed PSCAD model and final parameters are determined. The final MMC converter parameters are listed below:

SM type	Half-Bridge SM
Number of phases	3
Number of levels	20
Operating frequency	300 Hz
SM capacitance	250μF
Arm inductance	20mH
IGBT module	ABB 5SNA1300K450300
Modulation technique	NLM
Voltage balancing algorithm	MinMax algorithm
Processing resources	FPGA (ex. NI-RIO board)

The estimated weight and losses for LCL DC/DC converter with the above MMC parameters are calculated as:

Freq. (Hz)	Total Weight (Ton)	Total volume (m^3)	Total SMs power losses (MW)	Total LCL inductors conduction losses (MW)	Total Larm conduction losses (MW)	Total power losses (MW)	Total power losses (%)
300	721	619	14.6	0.39	0.18	15.17	1.52

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